

# **Statistical Analysis of Low Frequency Noise in Enclosed Gate MOSFETs**

## **Diploma Thesis**

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# Abstract

CMOS (Complementary Metal Oxide Semiconductor) technology continues to be the dominant technology for fabricating integrated circuits (ICs or chips), presenting advantages such as: reliability, low cost, low power consumption and most important scalability. Moore's Law which predicted that the number of devices on a chip will double every 18 to 24 months, fulfilled over the years by scaling down the feature size in CMOS technology. In early CMOS transistors the gate lengths were in micrometer range whereas the feature size of current CMOS devices is under 180nm. Nowadays, many integrated circuits are designed to operate in radiation environments such as aircraft, medical, space, nuclear applications and high energy physical experiments. Radiation total ionizing dose effects (TID) degrade the performance and reliability of MOS field effect transistors (MOSFETs), giving rise to positive charge trapping at the edges of shallow trench isolation (STI) corners, resulting to the formation of leakage current paths from drain to source diffusions. The use of transistors with enclosed gate layouts is the proposed solution for applications in radiation-hard (rad-hard) environments since due to their geometry and the absence of STI corners, there is no possible leakage current path along the edge of the active area. However, enclosed gate MOS devices present drawbacks like: increased area and limitations in the choice of the W/L ratio that should be taken into consideration.

The performance of conventional CMOS integrated circuits and designs that use enclosed gate transistors, can be limited by low frequency noise (LFN). In ultra-deep submicron technologies (UDSM) the impact of RTS (Random Telegraph Signal) noise is becoming a crucial factor for applications like multilevel-shell flash memories, CMOS image sensors and voltage controlled oscillators (VCOs). Generation-recombination noise (RTS noise) and flicker or  $1/f$  noise are the two main contributors forming low frequency noise (LFN) power spectral density (PSD) in low frequencies. RTS noise can be observed in small area MOS devices and is created by a trapping-de-trapping mechanism of free charges near the  $\text{SiO}_2/\text{Si}$  interface. Each trapping and de-trapping event associated with a single trap, give rise to a random telegraph signal (RTS) in time domain or a Lorentzian-like spectrum in frequency domain. In larger devices with large number of traps, due to uniform spatial trap distribution, the superposition of different Lorentzians will create a noise PSD inversely proportional to the frequency, typical of  $1/f$  noise.

In the context of this thesis, a detailed statistical analysis of low frequency noise in enclosed gate MOSFETs, in a 0.18 $\mu\text{m}$  CMOS process, was implemented for the first time. The results were evaluated under the carrier number fluctuation with correlated mobility fluctuations model. The bias-related and area-related LFN variability was also examined. Overall, this study leads to some interesting results. Enclosed gate NMOS devices show a higher variability than enclosed gate PMOS devices but lower noise levels. This is similarly as in standard transistors. On the other hand, enclosed gate PMOS devices, in weak inversion, show a reduce noise level at increased drain voltage. This noise reduction is interestingly accompanied by noise variability reduction.

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# Chapter 1

## Introduction

### 1.1 Noise impact on CMOS technology

Noise is generated in all semiconductor devices and is perceived as spontaneous random fluctuations in current or in voltage. In Metal Oxide Semiconductor Field Effect Transistors (MOSFETs), noise behavior is dominated primarily by two noise sources: thermal noise and low frequency noise (LFN) or  $1/f$  noise. Other noise sources that are sometimes present on the power spectrum of a MOS device are generation-recombination noise or random telegraph signal (RTS) noise and shot noise. Over the last years the aggressive reduction of the physical size of MOSFETs, established the use of CMOS technology in radio-frequency (RF) and high-speed integrated circuits (ICs). In analog design, noise determines the minimum AC signal that can be processed by an analog circuit whereas in applications like multilevel-shell flash memories, CMOS image sensors and voltage controlled oscillators (VCOs), the impact of RTS noise is crucial.

This thesis mainly focuses on Low Frequency Noise on transistors with enclosed gate layout. RTS noise and  $1/f$  noise are the two noise sources that compose the power spectral density of LFN, and they are associated with the trapping-de trapping mechanism of free charges at or near the  $\text{SiO}_2/\text{Si}$  interface, that is caused by structural defects. As mentioned above, noise can limit the performance of any CMOS application, especially in ultra-deep submicron technologies. Therefore, LFN measurements, characterization and modeling, are essential for noise behavior prediction in order to overcome its implications.

### 1.2 Thesis structure

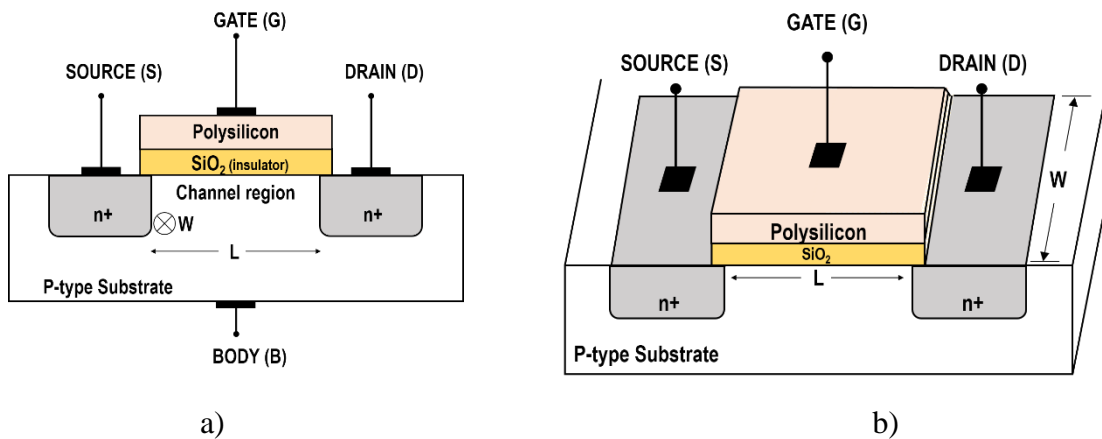
The context of this thesis is organized as follows: in this Chapter a brief introduction about noise impact on CMOS technology was presented. In Chapter 2, the basic MOSFETs structure and operation along with the special characteristics of MOSFETs with enclosed gate layout, will be demonstrated. In Chapter 3, Low Frequency Noise theory and the models that will be used for noise characterization, will be discussed in detail. In Chapter 4, the complete experimental process and results will be presented and analyzed. In Chapter 5 conclusions will be drawn.

# Chapter 2

## Device Structure & Physical Operation

### 2.1 Basic MOSFET structure

The MOS transistor is a field effect device, where the current flow in the longitudinal direction, from drain to source terminal in the region labeled as “channel region”, is modulated by the voltage applied at the gate [2, 4]. In Figure 2.1 the simplified structure of an NMOSFET is depicted. The four terminals of a MOSFET are: Gate (G), Source (S), Drain (D) and Body or Bulk (B). The transistor is fabricated in a p-type substrate silicon wafer, which provides physical support for the device, and consists of two heavily doped n-type diffusion regions, indicated in the figure as n+ drain and n+ source. The dimension of the gate along the source-drain path is called length  $L$ , whereas  $W$  is the width.

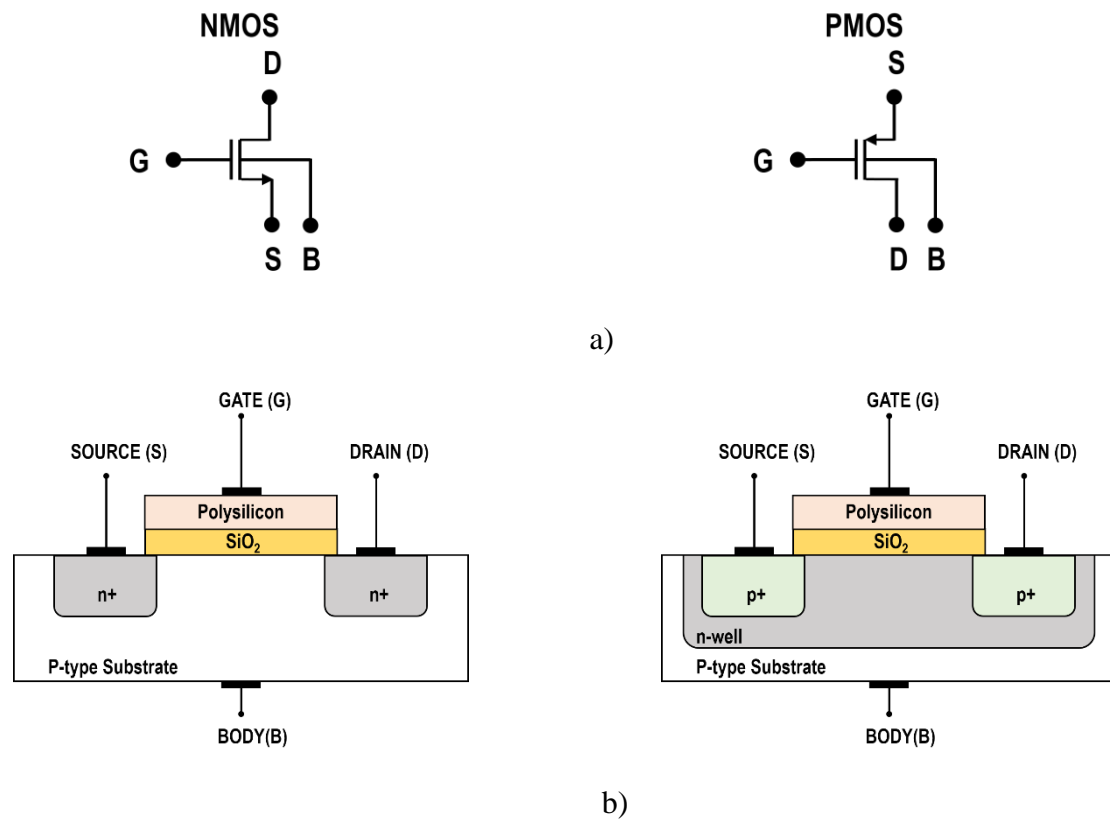


**Figure 2.1** a) Cross-Section of an n-type MOS Transistor, b) 3D perception of an NMOS device.

The surface between drain and source regions is covered with a thin layer of silicon dioxide (SiO<sub>2</sub>), which is an excellent electrical insulator, while a layer of polycrystalline silicon (or aluminum in older technologies) is deposited on top of the dielectric of the gate. The transistor structure is completely symmetrical with respect to source and drain. The role is defined by terminal voltages which establish the direction of carriers flow [2, 4].

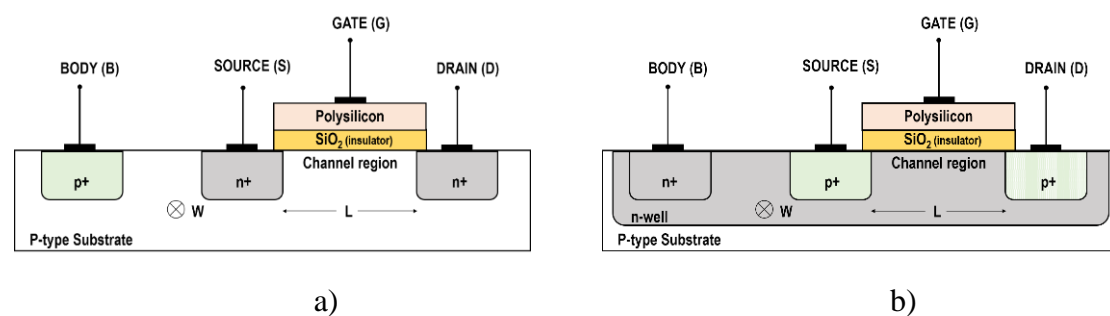
The PMOS transistor is a complementary structure to the NMOS transistor as depicted in Figure 2.2 b). P-type MOSFETs, have a similar structure with n-type MOSFETs and they are fabricated in the same substrate. They have opposite doping types, with p+ drain and p+ source diffusions placed in a local substrate called n-type

well. In a PMOSFET the minority carriers are the positive holes whereas in an NMOSFET the negative electrons [4].



**Figure 2.2** a) Circuit symbols, b) (left) Cross-Section of an NMOS device and (right) Cross-Section of a PMOS device.

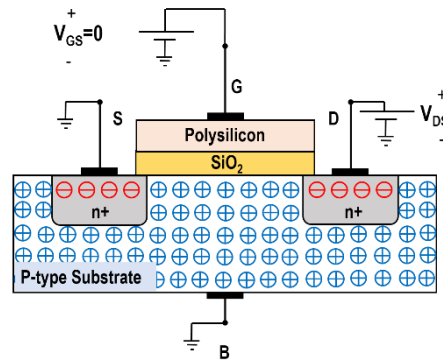
The potential of the substrate that the device is fabricated influences the device characteristics. In an NMOSFET the substrate is usually connected to the most negative supply of the system, usually the ground, and the actual connection is implemented through a p+ diffusion region, as illustrated in Figure 2.3 a). The n-type local substrate of a PMOSFET is tied to the most positive supply voltage through an n+ diffusion region (Figure 2.3 b) [2]).



**Figure 2.3** Substrate connection of a) an NMOSFET and b) a PMOSFET.

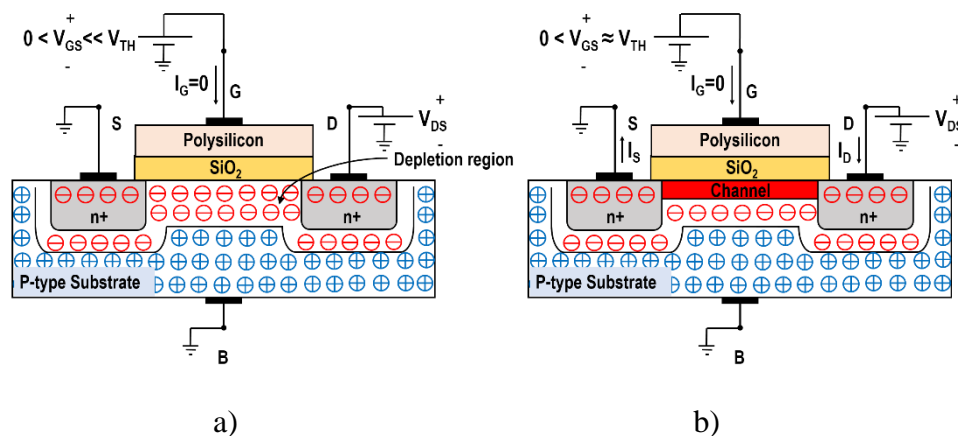
## 2.2 MOSFET Operation

In the operation with zero gate voltage ( $V_{GS}=0$ ), the two back-to-back diodes formed by the pn junctions between p-type substrate and n+ drain and n+ source regions, prevent current conduction from drain to source, when a voltage  $V_{DS}$  is applied (Figure 2.4).



**Figure 2.4** Cross-section of an NMOSFET on zero gate voltage operation.

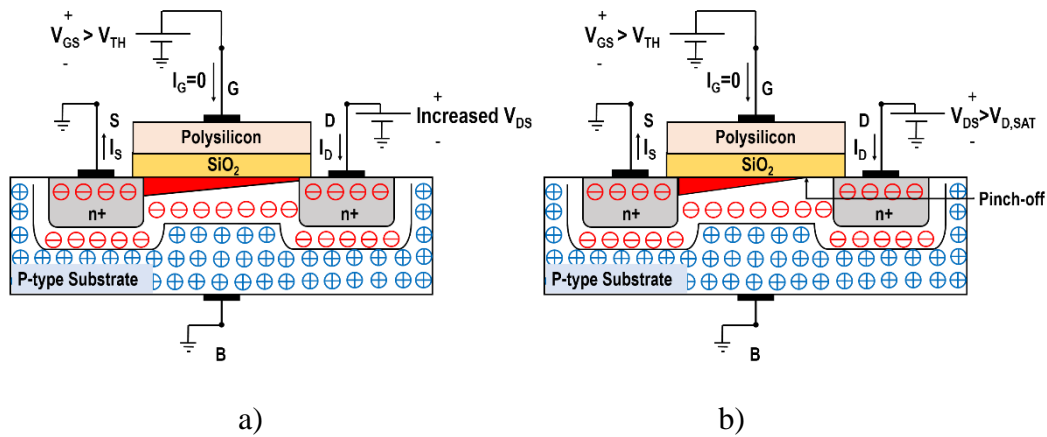
When gate voltage increases from zero ( $V_{GS}>0$ ), since gate and substrate form a capacitor (dielectric is SiO<sub>2</sub>), free holes are repelled from the substrate region under the gate leaving negative ions behind, thus a depletion region is formed (Figure 2.5 a)).



**Figure 2.5** a) Formation of depletion region and b) shaping of n-type channel.

As the gate voltage increases more, the width of the depletion region expands further and electrons are attracted from n+ drain and source areas, near the surface of the substrate under the gate oxide [4]. When the gate voltage approaches a sufficiently positive value called the threshold voltage ( $V_{GS} \approx V_{TH}$ ), an n-type channel of charge carriers, or inversion layer, is formed connecting drain and source regions. If a voltage

is applied between drain and source terminals ( $V_{DS} > 0$ ), current flows through this induced n-type region from drain to source (Figure 2.5 b)). For small values of the potential difference  $V_{DS}$ ,  $I_D$  value increases progressively with the increase of  $V_{DS}$  and the channel acquires a tapered shape at the drain end side (Figure 2.6 a)). The device operates in the “linear” region [2, 4]. When drain-source voltage exceeds a specific value called saturation value,  $V_{D,SAT}$ , the depth of the channel at the drain end approaches zero, the channel is pinched-off, drain current becomes relatively constant and the device operates in the “saturation” region (Figure 2.6 b)). In this operation region the device acts as a current source under control of the gate-source voltage.



**Figure 2.6** a) Linear region of MOSFET operation and b) channel pinch-off.

So far the basic operation of an NMOS device was demonstrated. A PMOS device, follows exactly the same operational characteristics with the difference that negative gate and drain voltages must be applied [2].

## 2.3 Regions of inversion

As described in the previous section gate voltage is responsible of forming the inversion layer, or channel, under the gate oxide, whereas the value of drain voltage defines two regions of operation linear and saturation. Additionally, depending on the value of the gate-source voltage, the MOSFET has two distinct physical regions of operation: weak (WI) and strong (SI) inversion. Between them there is a transition region known as moderate inversion (MI) [3].

In weak inversion the channel is weakly inverted and drain diffusion current dominates. This occurs when the device is operating at sufficiently low effective gate-source voltage ( $V_{EFF} = V_{GS} - V_{TH} \approx -72\text{mV}$ ) where the gate-source voltage is below the threshold voltage (sub-threshold region) by at least 72 mV. MOS weak inversion drain current in saturation is approximated by:

$$I_D(WI,SAT) = 2n\mu C_{ox}' U_T^2 \left( \frac{W}{L} \right) \left( e^{\frac{V_G - nV_S - V_{TH}}{n U_T}} \right) \quad (2.1)$$

where,  $n$  ( $n \approx 1.4$ ) is the substrate factor,  $\mu$  is the channel carrier mobility,  $C_{ox}'$  is the gate-oxide capacitance per unit area:

$$C_{ox}' = \epsilon_{SiO_2} / T_{ox} \quad (2.2)$$

and  $U_T$  the thermal voltage:

$$U_T = k T / q \quad (2.3)$$

where  $\epsilon_{SiO_2} = 3.45 \cdot 10^{-11}$  F/m is the permittivity of silicon dioxide,  $q = 1.602 \cdot 10^{-19}$  C is the magnitude of electron charge,  $T_{ox}$  is the oxide thickness which is determined by the process technology used to fabricate the MOSFETs ( $T_{ox} = 3.3$  nm for 0.18  $\mu$ m CMOS technology),  $k = 1.3086 \cdot 10^{-23}$  J/K is the Boltzmann's constant and  $U_T = 25.8$  mV at room temperature ( $T=300$  K).

When the gate-source voltage exceeds the threshold voltage by at least 225 mV, the channel is strongly inverted and drift current dominates [3]. At this point the device is operating in strong inversion. Drain current for strong inversion and saturation is defined as:

$$I_D(SI,SAT) = \frac{1}{2n} (\mu C_{ox}') \left( \frac{W}{L} \right) (V_G - nV_S - V_{TH})^2 \quad (2.4)$$

For the two different regions of inversion, weak inversion (WI) and strong (SI) inversion, the drain-source saturation voltage,  $V_{D,SAT}$ , can be calculated from the following equations:

$$V_{D,SAT}(WI) = 4U_T \quad (2.5)$$

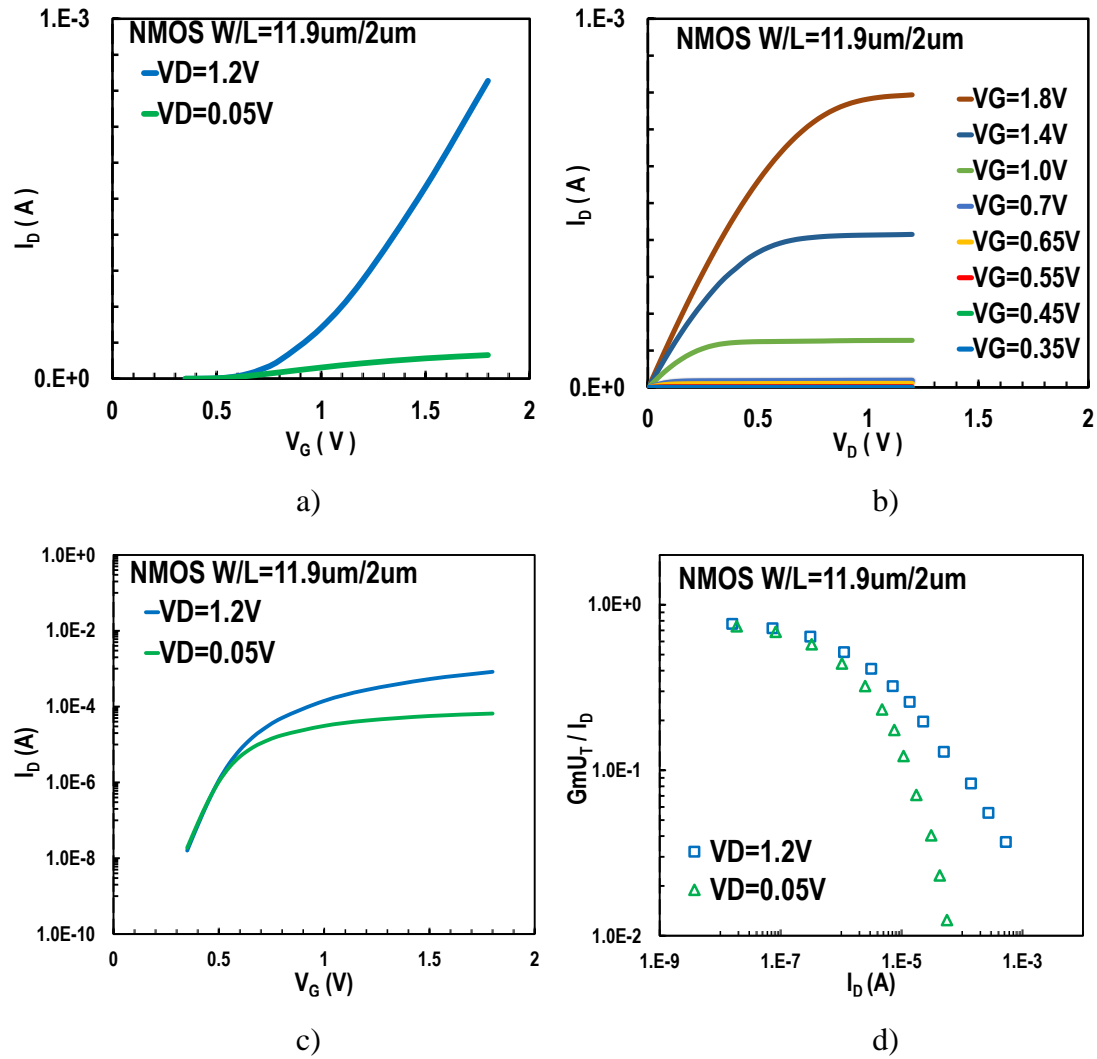
$$V_{D,SAT}(SI) = \frac{V_G - nV_S - V_{TH}}{n} \quad (2.6)$$

The drain current for both weak and strong inversion, in linear region of operation can be approximated from the following equation:

$$I_{D,LIN} \approx (\mu C_{ox}') \left( \frac{W}{L} \right) [V_G - V_{TH} - \frac{n}{2} (V_D + V_S)] \cdot (V_D - V_S) \quad (2.7)$$



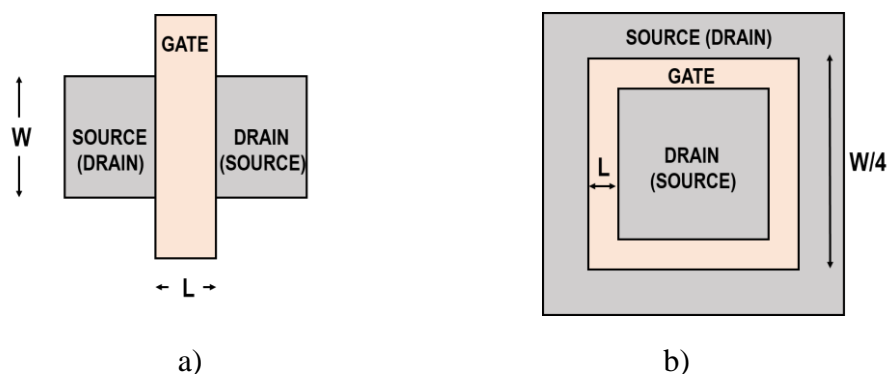
The typical  $I_D$  versus  $V_G$  and  $I_D$  versus  $V_D$  plots of a MOS device, also called transfer and output characteristics respectively along with  $G_m U_T / I_D$  versus  $I_D$  plot, are presented in Figure 2.6. In weak inversion  $I_D$  presents an exponential behavior while for each different  $V_G$  value, the drain current is saturated over a specific  $V_D$  value ( $V_{D,SAT}$ ) [2, 3, 4].



**Figure 2.7** a,c)  $I_D$  vs.  $V_G$  transfer and b)  $I_D$  vs.  $V_D$  output characteristics, and d)  $G_m U_T / I_D$  vs.  $I_D$ , of an NMOS transistor for both linear and saturation region of operation from weak to strong inversion. In c) y-axis is in logarithmic scale.

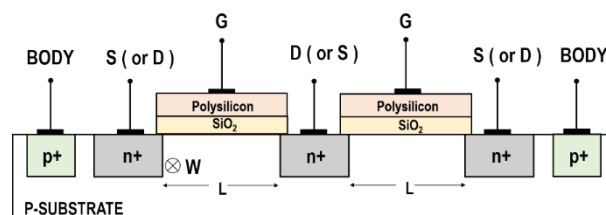
## 2.4 MOSFETs with enclosed gate layout

CMOS integrated circuits nowadays are widely used in many areas with high requirements for radiation resistance such as high energy physics, nuclear physics, aerospace and defense industry. Furthermore, as technology nodes scale down (under 0.18 $\mu\text{m}$ ), the impact of RTS (Random Telegraph Signal) noise is becoming a crucial factor in the performance of applications like multilevel-shell flash memories, CMOS image sensors, voltage controlled oscillators(VCOs) and mixers. In this section, a MOS transistor with a radiation hard topology and less vulnerable to RTS noise, due to the absence of STI corners, will be presented. In Figure 2.8 b) the basic layout of such a device, called enclosed gate MOSFET, is illustrated.



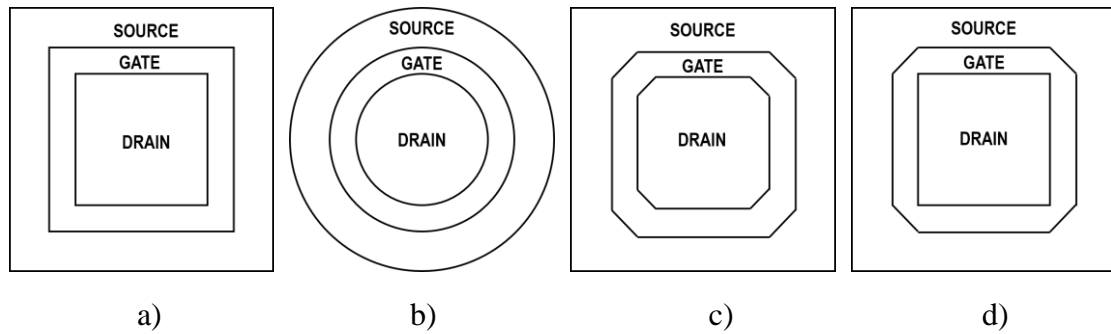
**Figure 2.8** a) Planar view of a standar MOSFET and b) an enclosed gate MOSFET.

In MOSFETs with enclosed gate layout the drain (or source) diffusion is fully surrounded by the gate polysilicon and the source (or drain) diffusion. The choice of the inner electrode as drain or source is defined by the bias voltage although as reported at [6] and [7] with the selection of the outer electrode as the drain, a device with an annular structure will exhibit lower drain electric fields and better reliability than a convetional one. On the other hand, if the inner electrode is selected as the drain, the substrate contact will be closer to the source and the drain resistance will be reduced resulting to higher output conductunce [6]. In Figure 2.9 a cross section of an enclosed gate n-type MOSFET is depicted [8].



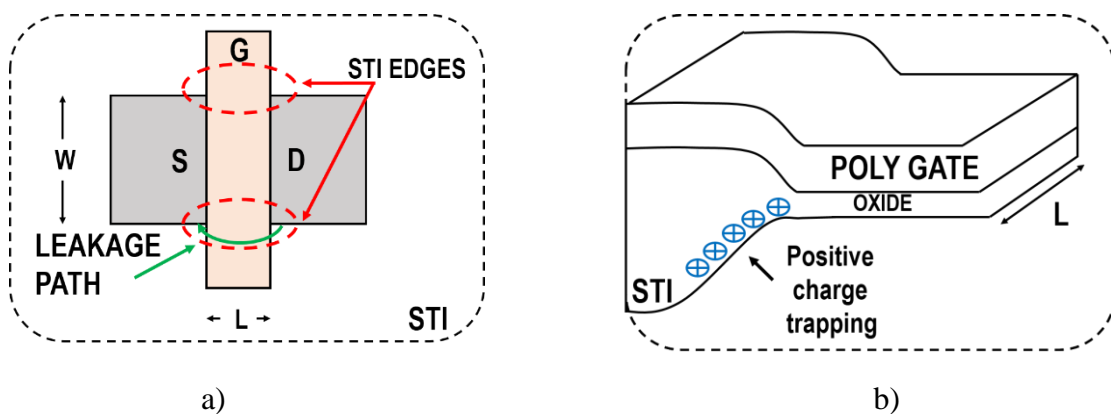
**Figure 2.9** Cross section of an enclosed gate NMOSFET with a p+ diffusion bulk connection.

Enclosed gate transistors come in a variety of different shapes. In Figure 2.10 some of the most widely used layouts like, square, circular, square with corners cut at  $45^\circ$  and square with  $45^\circ$  outer poly-edge cut, are presented [6,11]. In quarter-submicron process, due to design rules, neither circular layout nor  $90^\circ$  gate corners are possible to be manufactured, thus the shapes chosen are those with the  $45^\circ$  corners cut [6].



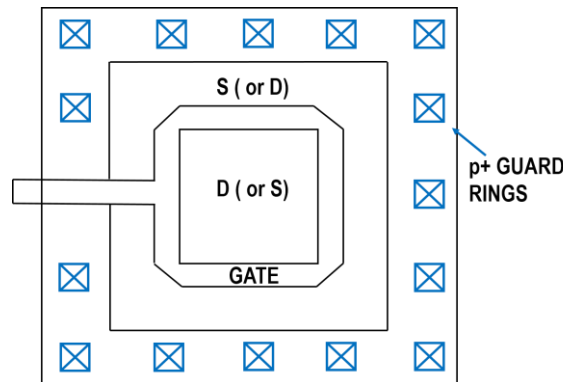
**Figure 2.10** Common enclosed gate MOSFET shapes. a)square, b)circular, c)octagonal and d) square with  $45^\circ$  outer poly-edge cut.

In conventional MOSFETs, techniques like STI (Shallow Trench Isolation) and LOCOS (Local Oxidation of Silicon) are used in order to provide better isolation between different devices and define the active silicon area. In radiation environments, due to positive charge trapping at the edges of STI corners (Figure 2.11b), or Bird's Beak region [13], an induced inversion layer will give rise to a transistor leakage current path from drain to source, as illustrated in Figure 2.11a). Enclosed gate MOSFETs without STI along with guard rings (Figure 2.12), can eliminate the edge leakage and



**Figure 2.11** a) Current leakage path in a conventional NMOSFET with STI and b) Bird's Beak region with trapped holes.

prevent leakage current between components. This can be realized because any current between source and drain has to flow underneath the gate oxide and there is no possible current path along the edge of the active area [11]. Additionally RTS noise, which is related to trapping sites within the gate oxide-silicon interface due to structural defects, can be affected by the presence of shallow trench isolation. During the STI process, the device



**Figure 2.12** Square NMOSFET with 45° outer poly-edge cut, p+ guard rings and polysilicon gate extension.

can be damaged at the STI boundary resulting to the generation of extra traps at the edge of the channel under the gate region [13]. As the device dimensions scales down the ratio of device gate edge to area increases and the STI edge effect dominates the overall RTS performance [9]. Since low frequency noise is strongly related to RTS noise, as will examined in detail in Chapter 3, devices without STI, like enclosed gate transistors, are expected to exhibit greatly improved  $1/f$  noise characteristics like lower drain current PSDs and lower relative current variations ( $\Delta I_D/I_D$ ) [10].

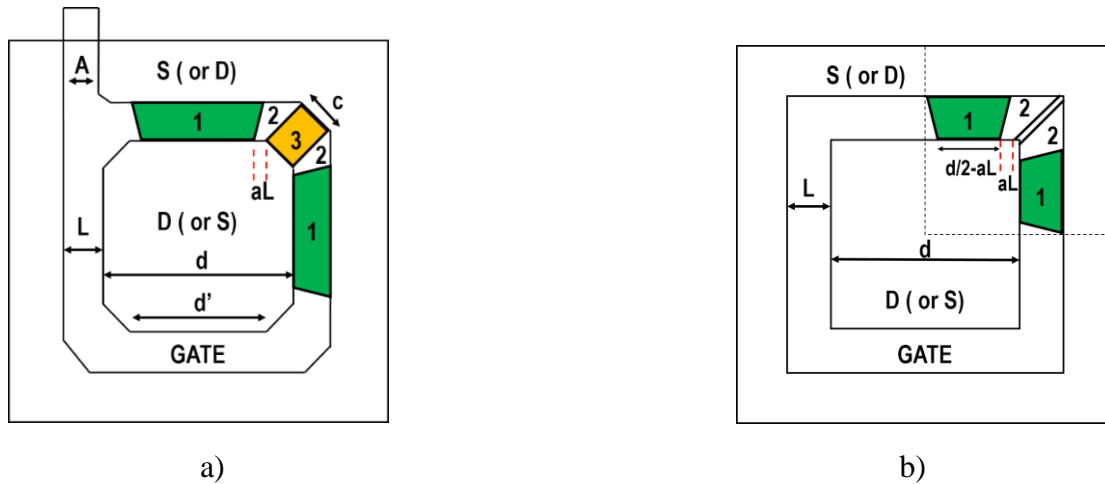
## 2.5 Modeling the W/L ratio in enclosed gate MOSFETs

Unlike the conventional MOSFETs in transistors with enclosed gate geometries the definition of the aspect ratio  $W/L$ , is not trivial. The extraction of the  $W/L$  values comes from the comparison of the  $I_D-V_{GS}$  characteristics between enclosed and standard devices with the same gate length ( $L$ ) [6]. For rectangular and square layouts, due to the distribution of the electric field in the corners of the gate, the transistor must be divided into smaller parts with the use of conformal mapping technique. These parts can be considered as smaller transistors contributing accordingly to the drain current of the MOSFET. Figure 2.13 shows the decomposition of a broken corner square and a square MOSFET into smaller transistors with 3 different basic shapes. Trapezium 1 is the approximation of the edge transistor, trapezium 2 corresponds to the corner

transistor and rectangle 3 is used to model the 45° edge cuts in the case of broken square corner MOSFET. The effective W/L ratio of a square MOSFET can be calculated from the equation [12]:

$$\left(\frac{W}{L}\right)_{\text{eff}} = 4 \frac{2a}{\ln(d'/d - 2aL_{\text{eff}})} + 2K \frac{1-a}{\frac{1}{2} \ln \frac{1}{a} \sqrt{a^2 + 2a + 5}} + 3 \frac{(d-d')/2}{L_{\text{eff}}} \quad (2.7)$$

where  $d' = d - c\sqrt{2}$  and  $a$  is a fitting parameter which is needed to identify the borders between transistors 1 and 2. For different CMOS technologies scaling from 2.5μm to 0.25 μm,  $a$  has been found to be almost technology independent with a value of 0.05. Parameter  $K$  is geometry dependent with a value of 7/2 for devices with  $L \leq 0.5\mu\text{m}$  and 4 for longer devices [6, 12].



**Figure 2.13** a) Square and b) broken corner square MOSFET formed by different types of transistors in parallel.

Under the same approach, the aspect ratio of the square layout is given by [6]:

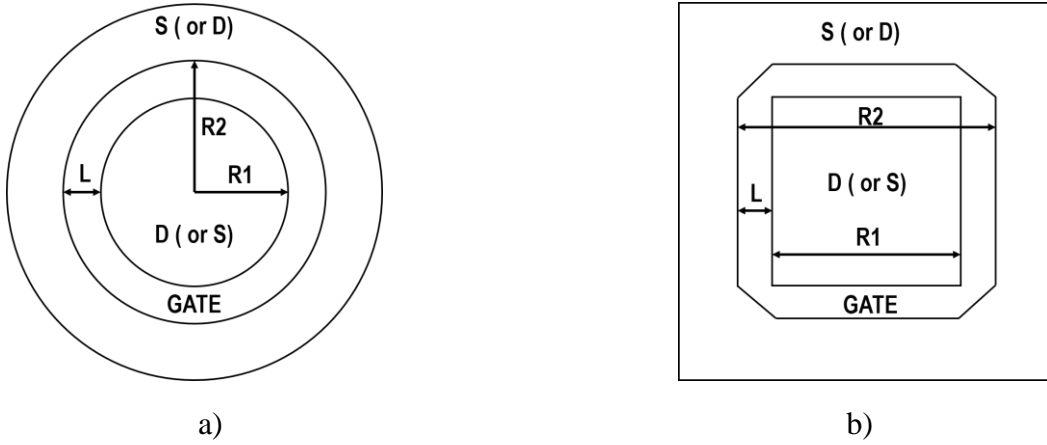
$$\left(\frac{W}{L}\right)_{\text{eff}} = 4 \cdot 2 \left( \frac{a}{\ln(d/d - 2aL_{\text{eff}})} + \frac{1}{\frac{1}{2} \sqrt{a^2 + 2a + 5}} - \frac{(1-a)}{-\ln a} \right) \quad (2.8)$$

Again  $a=0.05$  can be chosen to assure a good W/L predictability. It should be noticed that the only way to achieve lower aspect ratios is to increase  $L$  and keep  $d$  constant. Therefore, transistors with enclosed gate layouts, cannot have aspect ratios lower than a certain value [6, 12].

For enclosed gate MOSFETs with circular geometry the effective W/L ratio can be approximated by the following equation:

$$\left(\frac{W}{L}\right)_{\text{eff,CIRC}} = \frac{2\pi}{\ln(R2/R1)} \quad (2.9)$$

where R1 is the inner diffusion radius and R2=L+R1. In this case if the drain radius is greater than the channel length (L<< R1) the above equation gives a very good approximation of the effective W/L ratio whereas for long channel devices overestimates the result [6].



**Figure 2.14** a) Circular and b) square with 45° outer poly-edge cut MOSFETs.

For square transistors with 45° outer polysilicon-edge cut (Figure 2.10b), a more compact approach of the effective W/L ratio is given by:

$$\left(\frac{W}{L}\right)_{\text{eff,OUTERCUT}} = \frac{8}{\ln(R2/R1)} \quad (2.10)$$

where R1 is the inner diffusion length, L is the channel length and R2=R1+L [11].

As mentioned above, transistors with enclosed gate layout, can prevent current leakage in irradiated circuits and exhibit improved low frequency noise characteristics. However, drawbacks like: consumption of area, limitations in the choice of the W/L ratio, and difficulties in modeling the W/L ratio should be mentioned.

# Chapter 3

## Low-Frequency noise in MOSFETs

### 3.1 Noise

Noise can be described as random and uncorrelated fluctuations of a signal. Consequently, an instantaneous noise value is unpredictable even if past values are known [2]. Observation of noise and use of measured results for constructing a statistical model is the solution in order to incorporate noise to circuit and electronic device analysis. In time domain, noise can be described by the average noise power ( $P_{av}$ ) while in frequency domain by the Power Spectral Density (PSD). The average power of a noise waveform  $x(t)$  is given by [2, 5]:

$$P_{av} = \lim_{T \rightarrow \infty} \frac{1}{T} \int_{-T/2}^{+T/2} x(t)^2 dt \quad (3.1)$$

and is expressed in  $V^2$  or Watt. The spectrum (PSD) shows how much power a signal carries at each frequency and can be defined as:

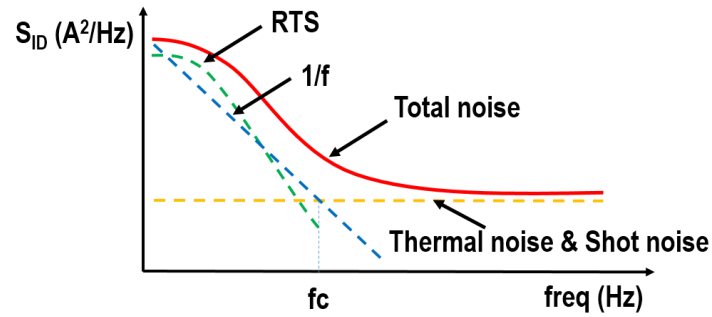
$$S(f) = \lim_{T \rightarrow \infty} \frac{|X(f)|^2}{T} \quad (3.2)$$

$S(f)$  is expressed in  $V^2/Hz$  or Watt/Hz and  $X(f)$  is the Fourier transform of the noise waveform  $x(t)$  [5].

### 3.2 Noise in MOSFETs

Noise is generated in all semiconductor devices and is perceived as spontaneous random fluctuations in current or in voltage. In MOSFETs, there are several noise mechanisms coming from the channel of the device, related to local random fluctuations of the carrier velocity or the carrier density and they are observed over various frequency ranges [1]. Specifically, noise sources are: Thermal noise, low frequency noise (LFN) or  $1/f$  noise, generation-recombination noise (RTS) and Shot noise. The total noise is thus a superposition of all noise components. In Figure 3.1 the expected pattern of the drain-referred noise current PSD is depicted. Thermal noise has no dependence on frequency and so is flat across the entire spectrum while low frequency

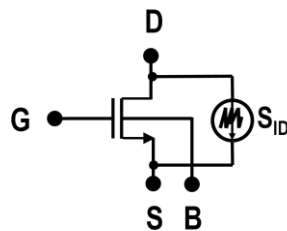
noise, comes with a power spectra density inverse proportional to the frequency [3, 14 15] and is dominant in frequencies lower than the corner frequency ( $f_c$ ), where thermal noise and LFN have equal PSDs. Low frequency noise consists of  $1/f$  noise and in smaller devices from RTS noise, whereas shot noise is flat across the spectrum.



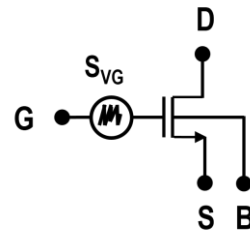
**Figure 3.1** Typical drain-referred noise current PSD of a MOSFET.

Both thermal and low frequency noise can be treated as drain-referred noise current or gate-referred noise voltage sources as illustrated in Figure 3.2. As mentioned

**Drain-referred noise current**



**Gate-referred noise voltage**



**Figure 3.2** MOSFET noise modeled as drain-referred noise current source or gate-referred noise voltage source.

above, noise sources are more often described by their power spectral density (PSD). The expressions used for the PSD conversion between drain-referred and gate-referred noise sources are:

$$S_{ID} = S_{VG} g_m^2 \quad (\text{A}^2/\text{Hz}) \quad (5.1)$$

$$S_{VG} = S_{ID} / g_m^2 \quad (\text{V}^2/\text{Hz}) \quad (5.2)$$

Quantity  $g_m$  is the gate conductance in Siemens (Appendix A.1).



### 3.3 Thermal Noise

Thermal noise in a resistive element is caused by random motion of carriers due to thermal excitation and introduces voltage fluctuations, in the voltage measured across the element, even if the average current is zero [2, 3]. Thermal noise sometimes called Johnson or Nyquist noise and because of its constant PSD with frequency also called “white noise”. Resistor thermal noise voltage PSD is given by:

$$S_{VG}(f) = 4kTR \text{ (V}^2/\text{Hz)} \quad (3.3)$$

where  $k$  is the Boltzmann’s constant (J/K),  $T$  is the absolute temperature (K) and  $R$  the resistance value (Ohm). MOSFETs also exhibit thermal noise generated from the channel area and can be related to the total inversion layer charge as described in the following equation:

$$S_{ID,THERMAL} = 4kT \frac{\mu_{eff}}{L^2} |Q_{inv}| \text{ (A}^2/\text{Hz)} \quad (3.4)$$

Here,  $\mu$  is assumed constant at  $\mu_{eff}$ ,  $T$  is the temperature,  $L$  is the channel length and  $Q_{inv}$  is the total inversion layer charge. A more practical approximation of the thermal noise power spectral density, valid for both saturation and linear regions of a MOSFET is given by:

$$S_{ID,THERMAL}(LIN,SAT) = 4kT \Gamma g_{ms} \text{ (A}^2/\text{Hz)} \quad (3.5)$$

where  $\Gamma$  is 1/2 in weak inversion and 2/3 in strong inversion [3]. The total source conductance is given by  $g_{ms}=g_m+g_{mb}+g_{ds}$ .

### 3.4 Shot Noise

Shot noise does not depend on frequency, and results from the random arrival of discrete carriers across a pn junction. The PSD of shot noise associated with the DC drain current of a MOSFET is expressed by:

$$S_{ID,SHOTNOISE} = 2qI_D \text{ (A}^2/\text{Hz)} \quad (3.6)$$

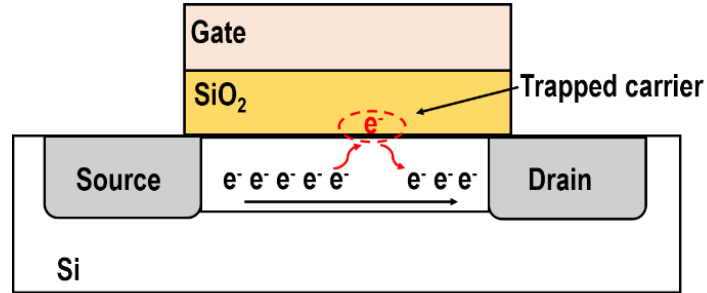
Equation 3.5, if we assume operation in saturation and weak inversion, where  $g_{ds}$  is negligible,  $\Gamma=1/2$  and  $g_m=I_D/(nU_T) = I_D/(nkT/q)$ , can be written as:

$$S_{ID,THERMAL}(WI,SAT) = 4kT n \Gamma g_m = 4kT n \frac{1}{2} \frac{I_D}{n \left(\frac{kT}{q}\right)} = 2qI_D \quad (3.7)$$

which means that under this conditions (SAT,WI) thermal noise and shot noise have the same power spectral density [3].

### 3.5 Generation-Recombination Noise (RTS noise)

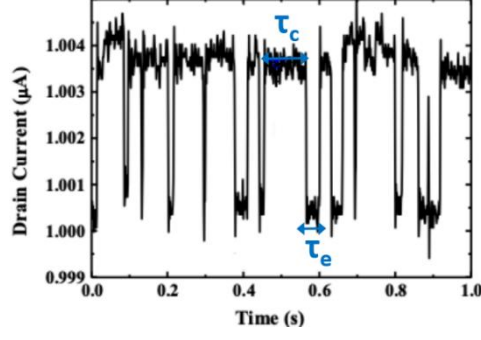
Generation-recombination noise in MOSFETs is correlated to trapping sites either within gate oxide or gate oxide-silicon interface. Carrier traps emerge from local defects of the  $SiO_2$  near the silicon substrate due to fabrication imperfections and introduce a trapping-de trapping mechanism of free charges at or near the  $SiO_2/Si$  interface [3, 14, 15, 17].



**Figure 3.3** MOSFET cross section showing a trapped carrier near Si-SiO<sub>2</sub> interface.

In a simplified approach, as depicted in Figure 3.3, because of a trap presence in the oxide a free carrier can be displaced from the channel for a short time period and then emitted back.

Structural defects are caused by dangling bonds of silicon atoms that are not bounded to other oxygen or silicon atoms. This lattice discontinuity creates energy levels in the bandgap of the semiconductor acting as generation recombination centers or traps [23]. Each trapping and de-trapping event associated with a single trap, give rise to a random telegraph signal (RTS) in time domain [10] as depicted in Figure 3.4. An RTS exhibits two discrete levels. The upper level corresponds to an empty trap, where  $\tau_c$  denotes the average time it takes to capture a carrier, while the lower level to an electron occupied state, with  $\tau_e$  to be the average time needed to release the carrier.

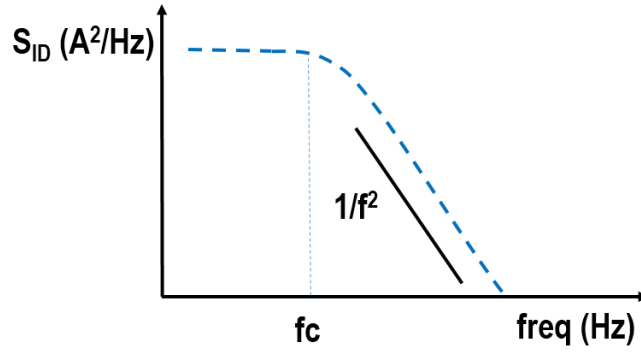


**Figure 3.4** Random telegraph signal in time domain.

Under this approach each trap is characterized by a time constant  $\tau$  that is calculated from the following equation [17]:

$$\frac{1}{\tau} = \frac{1}{\tau_c} + \frac{1}{\tau_e} \quad (3.8)$$

RTS are observed in small area MOS devices and they have a Lorentzian frequency spectrum as shown in Figure 3.5. A Lorentzian power spectrum is characterized by a constant power spectral density at low frequencies and a roll-off with  $f^{-2}$  at frequencies higher than the corner frequency  $f_c$  [15, 17].



**Figure 3.5** Typical Lorentzian power spectrum of an RTS.

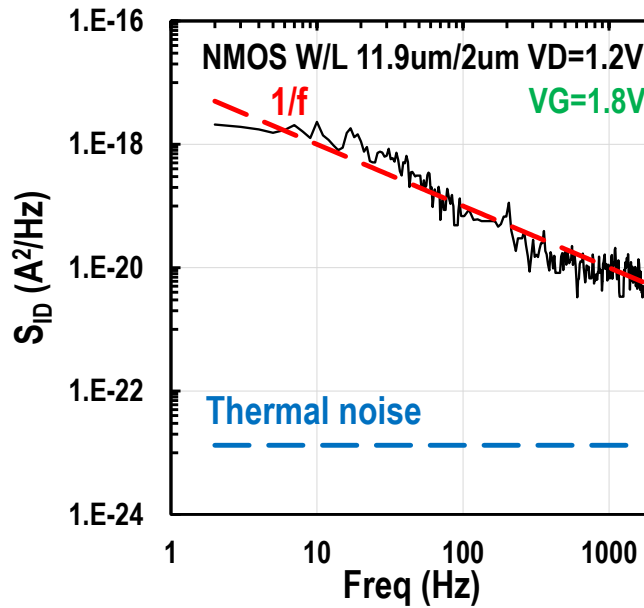
The Lorentzian power spectrum is given by:

$$S_{ID} = \frac{A}{\left(1 + \frac{f}{f_c}\right)^2} \quad (A^2/Hz) \quad (3.9)$$

where A is the amplitude factor and  $f_c$  the roll-off frequency.

### 3.6 Flicker Noise

Flicker noise or “1/f” noise is characterized by a PSD that is inversely proportional to frequency and dominates in low frequencies. Because the 1/f noise scales inversely proportional to the gate area and varies significantly across processes and process generations it is becoming a major issue for analog IC design in deep submicron devices. In Figure 3.6 the measured drain referred noise PSD of an enclosed gate NMOSFET is illustrated. Here the clear 1/f behavior of noise can be observed over



**Figure 3.6** Measured noise  $S_{ID}$  vs frequency, for an enclosed gate NMOSFET with  $W=11.9\mu m$  and  $L=2\mu m$ , at saturation region of operation ( $V_D=1.2V$ ) for  $V_G=1.8V$ .

a specific frequency range until the point that the PSD becomes flat, beyond the so called corner frequency  $f_c$ , where flicker noise “meets” thermal noise. At this point it is necessary to state that the PSD of flicker noise is actually proportional to  $1/f^{AF}$  where the exponent AF ranges between 0.7 and 1.2 [3].

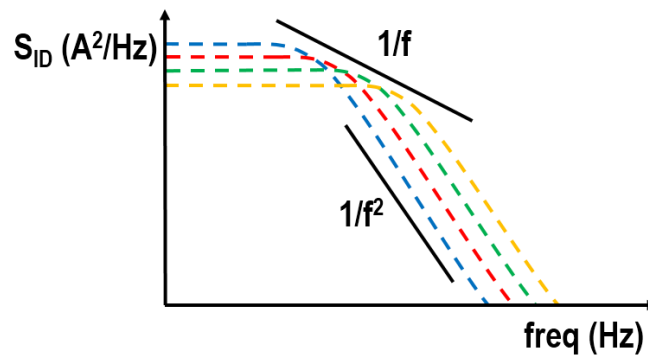
The basic causes of flicker noise are; carrier number fluctuation, carrier mobility fluctuation and series resistance fluctuation. In literature, the most common equation describing the gate-referred flicker noise voltage PSD is:

$$S_{VG,FLICKER} = \frac{K_F}{C_{OX}^2 W L^{AF}} (V^2/Hz) \quad (3.10)$$

$K_F$  is the flicker noise factor having units of  $C^2/cm^2$ , and  $AF$  is the frequency exponent, which has been added to consider the deviation from the ideal  $1/f$  slope.  $K_F$  typical values ranging from  $10^{-33}$  to  $10^{-29} C^2/cm^2$  [3].

### 3.7 Carrier number fluctuation model with correlated mobility fluctuations

Carrier number fluctuation model, also known as McWorther model or  $\Delta_N$  model, describes flicker noise as a result of free carriers trapping and de-trapping near the Si-SiO<sub>2</sub> interface and it is strongly correlated to the generation-recombination (RTS) noise process. As mentioned earlier, every single trap will modulate the total drain current with a Lorentzian spectrum which is characterized by a specific roll-off frequency. Shallower traps will lead to shorter time constants and higher roll-off frequencies while deeper traps to longer time constants and lower roll-off frequencies [17]. A uniform spatial trap distribution, will result to uniformly distributed time constants and therefore the superposition of different Lorentzians will create a PSD inversely proportional to the frequency, typical of  $1/f$  noise [16]. In Figure 3.7 a simplified approach of this mechanism is represented.



**Figure 3.7** Superposition of Loentzians forming the  $1/f$  slope of flicker noise.

In addition to the resulting carrier number fluctuation associated with the McWorther model, the so-called correlated mobility fluctuation model (CFM) suggests that both carrier density and mobility fluctuate as a result of the exchange of carriers between the channel and the gate dielectric. The latter is known as Coulomb scattering effect caused by trapping and de-trapping of free carriers. Under the unified carrier number fluctuation with correlated mobility fluctuations model, low frequency noise can be described adequately by the following equation [14, 15]:

$$\frac{S_{ID}}{I_D^2} = S_{Vfb} \left( \frac{g_m}{I_D} \right)^2 \left[ 1 + \alpha_c \mu C_{ox} \frac{I_D}{g_m} \right]^2 \quad (3.11)$$

where  $\alpha_c$  is the Coulomb scattering coefficient in  $VsC^{-1}$  and  $\mu$  the effective carrier mobility. The flat-band voltage spectral density,  $S_{Vfb}$ , is given by [14]:

$$S_{Vfb} = \frac{kTq^2 N_T \lambda}{C_{ox}^2 W L f} \quad (3.12)$$

where  $N_T$  is the volumetric trap density per unit in  $cm^{-3}eV^{-1}$ ,  $f$  is the frequency,  $kT$  is the thermal energy and  $\lambda$  is the tunneling attenuation distance ( $\sim 0.1$  nm for  $SiO_2$ ). The number of traps per unit area and in  $cm^{-2}$  can be calculated by the following equation:

$$N_t = N_T \lambda kT \quad (3.13)$$

$N_T$  parameter typical values varying from  $1.5 \cdot 10^{14}$  to  $1.5 \cdot 10^{18}/eVcm^3$ , depending on the process, whereas  $\alpha_c$  has approximate values  $10^4 VsC^{-1}$  for NMOSFETs and  $10^5 VsC^{-1}$  for PMOSFETs [3, 14].

### 3.8 Low-Frequency Noise variability

Low-Frequency Noise variability is strongly related with the statistical deviation of parameters  $N_T$  and  $\alpha_c$  that described above in equations 3.11 and 3.12 under the carrier number fluctuation model. In Small area devices with low number of traps RTS noise can be observed, resulting to an increased flicker noise dispersion. Parameter  $N_T$  follows Poisson statistics and is responsible for increasing noise variability in smaller devices. The relative standard deviation of traps number is given by [15]:

$$\sigma_{NT} = \frac{1}{\sqrt{N_t W L}} \quad (3.14)$$

On the other hand low frequency noise variability dependence with gate voltage can be described with parameter  $\alpha_c$ . In subthreshold region the inversion charge is non-uniform leading to bigger impact of trap location on  $\alpha_c$  parameter resulting to an increased noise dispersion [15]. The Low-Frequency noise model that describes both area-dependence and bias-dependence of  $1/f$  noise variability can be expressed by equation:

$$\sigma \left[ \log_{10} \left( WL \cdot \frac{SI_D}{I_D^2} \cdot f \right) \right] = \sqrt{B^2 \frac{gmU_T}{I_D} + \frac{A^2}{WL}} \quad (3.15)$$

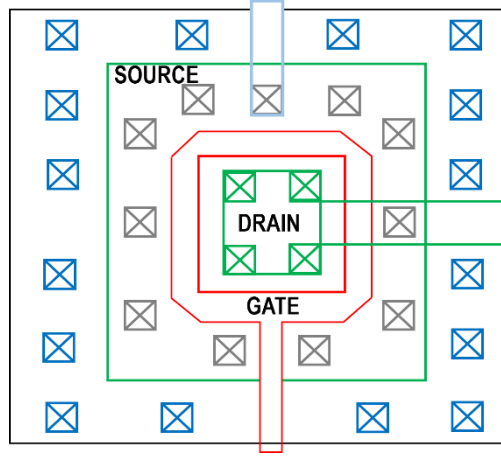
where  $A = 1/\sqrt{Nt}$  (area-related) and  $B = \alpha_c \mu Q_{\text{speq}}$  (bias-related) are the statistical model parameters, and  $Q_{\text{speq}}$  is the specific charge. The term  $gmU_T/I_D$  maximizes noise variability in weak inversion for moderated and large-area devices [15]. At this point it is necessary to report that the variance of 1/f noise has log-normal distribution and that is why the  $\log_{10} (WL \cdot f \cdot SI_D/I_D^2)$  expression is used.

# Chapter 4

## Experimental process and Results

### 4.1 Device under test and measurement setup

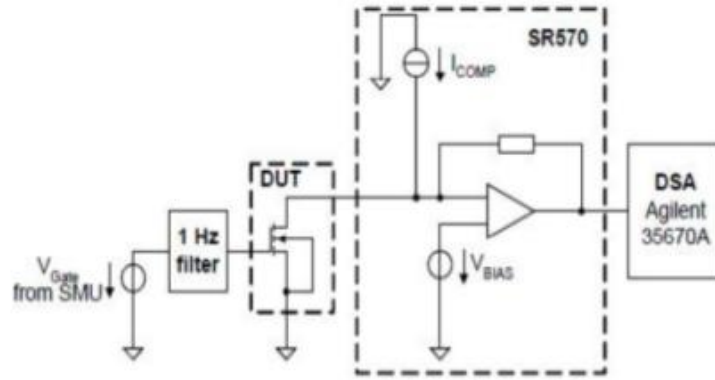
For the scope of this thesis on-wafer 1/f noise measurements on both PMOS and NMOS transistors with enclosed gate geometry, in a 0.18 $\mu\text{m}$  CMOS process from EM, where performed. The device tested, as illustrated on Figure 4.1, is a square MOSFET with outer polysilicon-edge cut, a fixed drain size of 1.4x1.4  $\mu\text{m}^2$  and no shallow trench isolation.



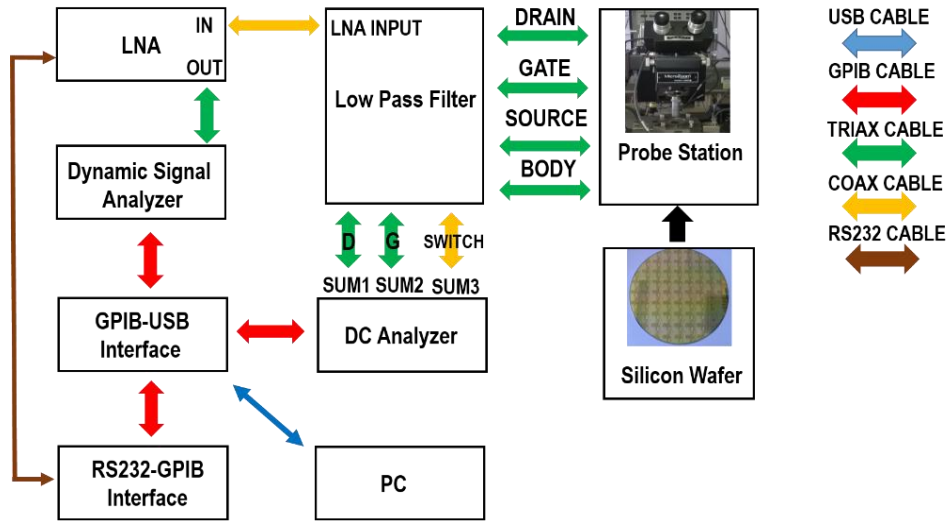
**Figure 4.1** Square n-channel MOSFET with outer polysilicon-edge cut, 4 drain contacts, 11 source, contacts, p+ guard rings, without STI and 1.4x1.4 $\mu\text{m}^2$  drain size.

The experiment was performed on a population of 30 PMOS and 50 NMOS devices, coming from 15 and 25 different wafer dies accordingly. For PMOS devices, transistors of  $W/L=11.9\mu\text{m}/2\mu\text{m}$ ,  $7.42\mu\text{m}/0.5\mu\text{m}$ ,  $6.87\mu\text{m}/0.34$  and  $6.29\mu\text{m}/0.18\mu\text{m}$  where measured at gate voltage values from weak to strong inversion region ( $|V_{GS}| = 0.45, 0.5, 0.55, 0.6, 0.7, 0.8, 1.0, 1.2, 1.5$  and  $1.8\text{V}$ ) and drain voltage values for both linear and saturation regions ( $|V_{DS}| = 0.05, 0.3$  and  $1.2\text{V}$ .  $1.2\text{V}$  for saturation region.). For NMOSFETs two different geometries where tested with,  $W/L=11.9\mu\text{m}/2\mu\text{m}$  and  $6.29\mu\text{m}/0.18\mu\text{m}$ , at gate voltage values:  $|V_{GS}| = 0.35, 0.4, 0.45, 0.5, 0.55, 0.6, 0.7, 0.8, 1.0, 1.2, 1.5, 1.8\text{V}$  (for  $L=0.18\mu\text{m}$ ) and  $|V_{GS}| = 0.35, 0.4, 0.45, 0.5, 0.55, 0.6, 0.65, 0.7, 0.8, 1.0, 1.2, 1.5, 1.8\text{V}$  (for  $L=2\mu\text{m}$ ), for both linear and saturation regions ( $|V_{DS}| = 0.05$  and  $1.2\text{V}$ .  $1.2\text{V}$  for saturation region.).





a)

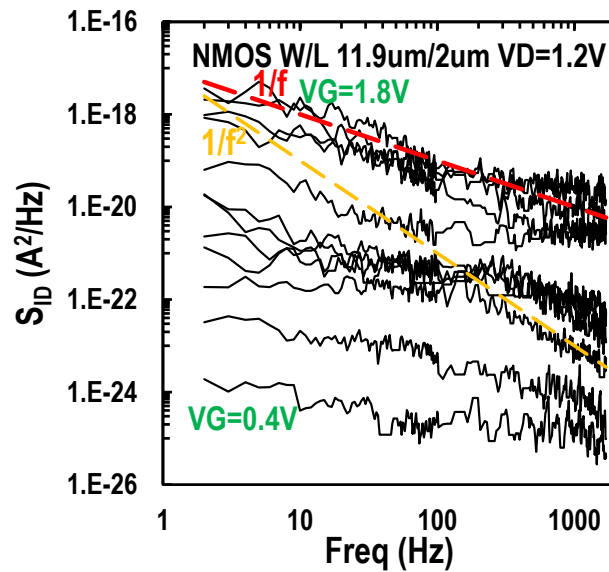


b)

**Figure 4.2** Low-Frequency noise set-up a) circuit diagram and b) block diagram with cable connections.

The on-wafer measurements set-up [17], as illustrated in Figure 4.2b, consists of: a Cascade Microtech Probe Station, a Stanford Research SR570 Low Noise Amplifier, a Low Pass Filter at 1 Hz, an Agilent 35670 Dynamic Singnal Analyzer, an HP4542A DC Analyzer , a GPIB-USB interface and a NI CV232A RS232-GPIB interface. The software used for measurements was Agilent ICCAP and the software intrface for I/V and noise measurements was provided by AdMOS. Further process of all the acquired data was implemented on Microsoft Office Excel 2013.

The experimental procedure for every device started with I/V measurements in order to export the basic output and transfer characteristics. Then, through AdMOS noise measurement software interface, the drain referred noise power spectral density for every device was extracted, at a frequency range from 2 to 1702 Hz, for all the gate voltage and drain voltage values that mentioned above. In Figure 4.3 the drain current noise PSD of an NMOSFET with  $W=11.9\text{ }\mu\text{m}$  and  $L=2\text{ }\mu\text{m}$ , for different gate voltage values, in saturation region of operation ( $V_{DS}=1.2\text{V}$ ), is illustrated. As we can observe lower

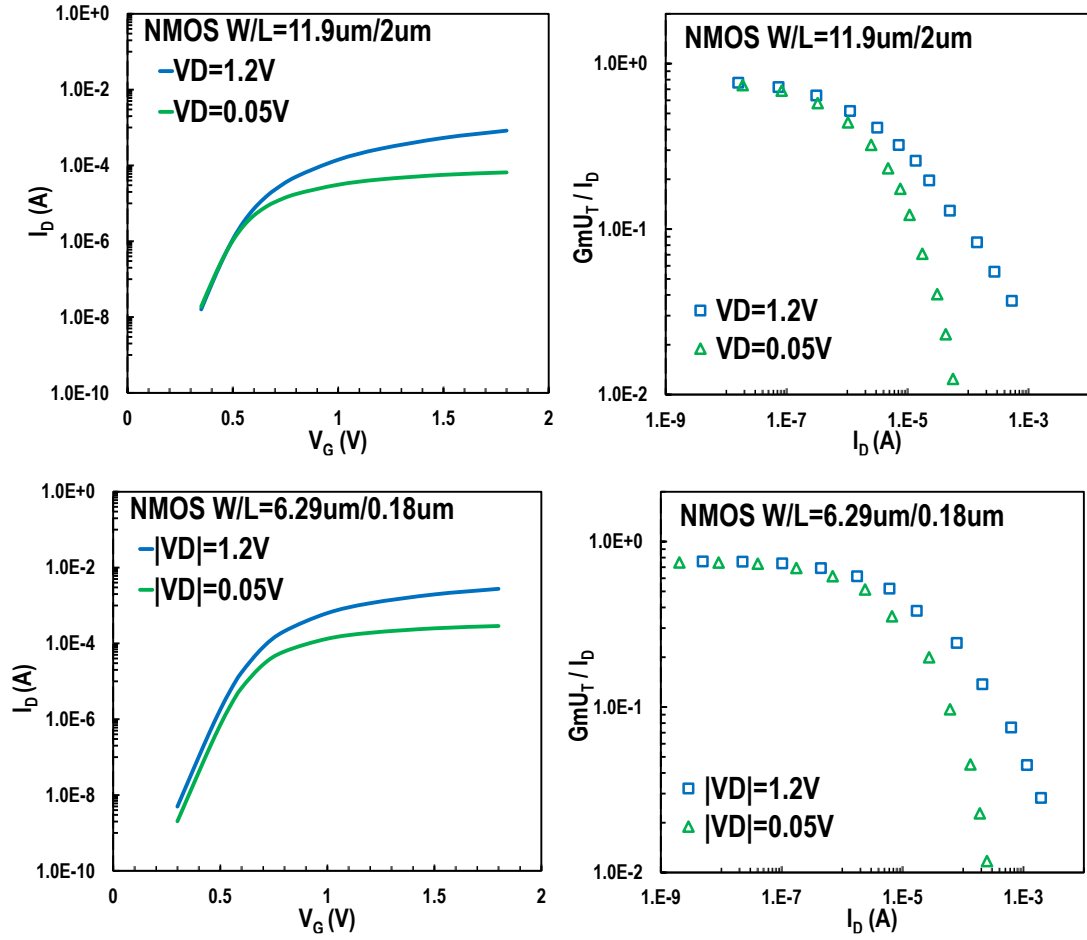


**Figure 4.3** Measured noise  $S_{ID}$  vs. Freq. for an NMOSFET with  $W/L=11.9\text{ }\mu\text{m}/2\text{ }\mu\text{m}$  from weak to strong inversion ( $V_{GS} = 0.4, 0.45, 0.5, 0.55, 0.6, 0.65, 0.7, 0.8, 1.0, 1.2, 1.5$  and  $1.8\text{V}$ ) at saturation region ( $V_{DS}=1.2\text{V}$ ).  $1/f$  and  $1/f^2$  trend lines are also depicted.

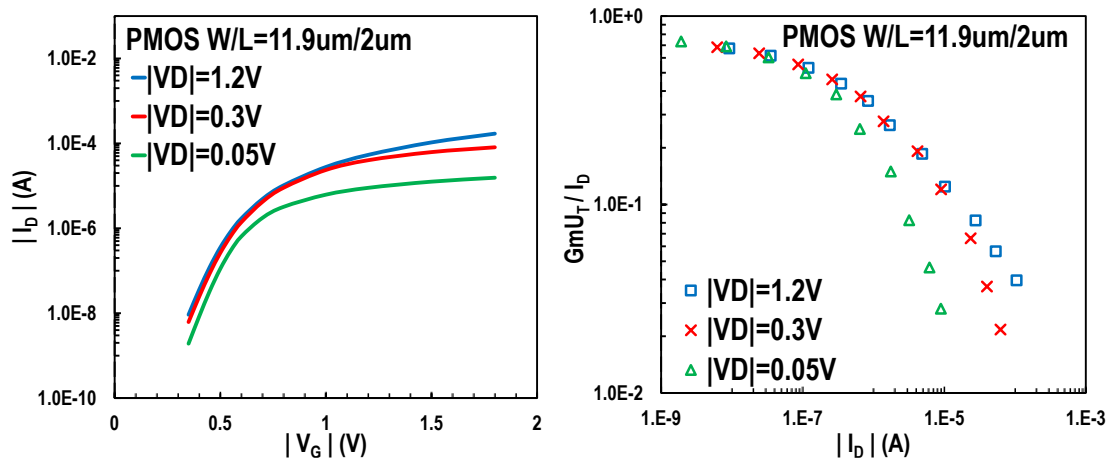
inversion level results to lower current noise PSD and lower corner frequency  $f_c$ . Furthermore, the clear  $1/f$  behavior of noise can be detected at frequencies lower than 100Hz.

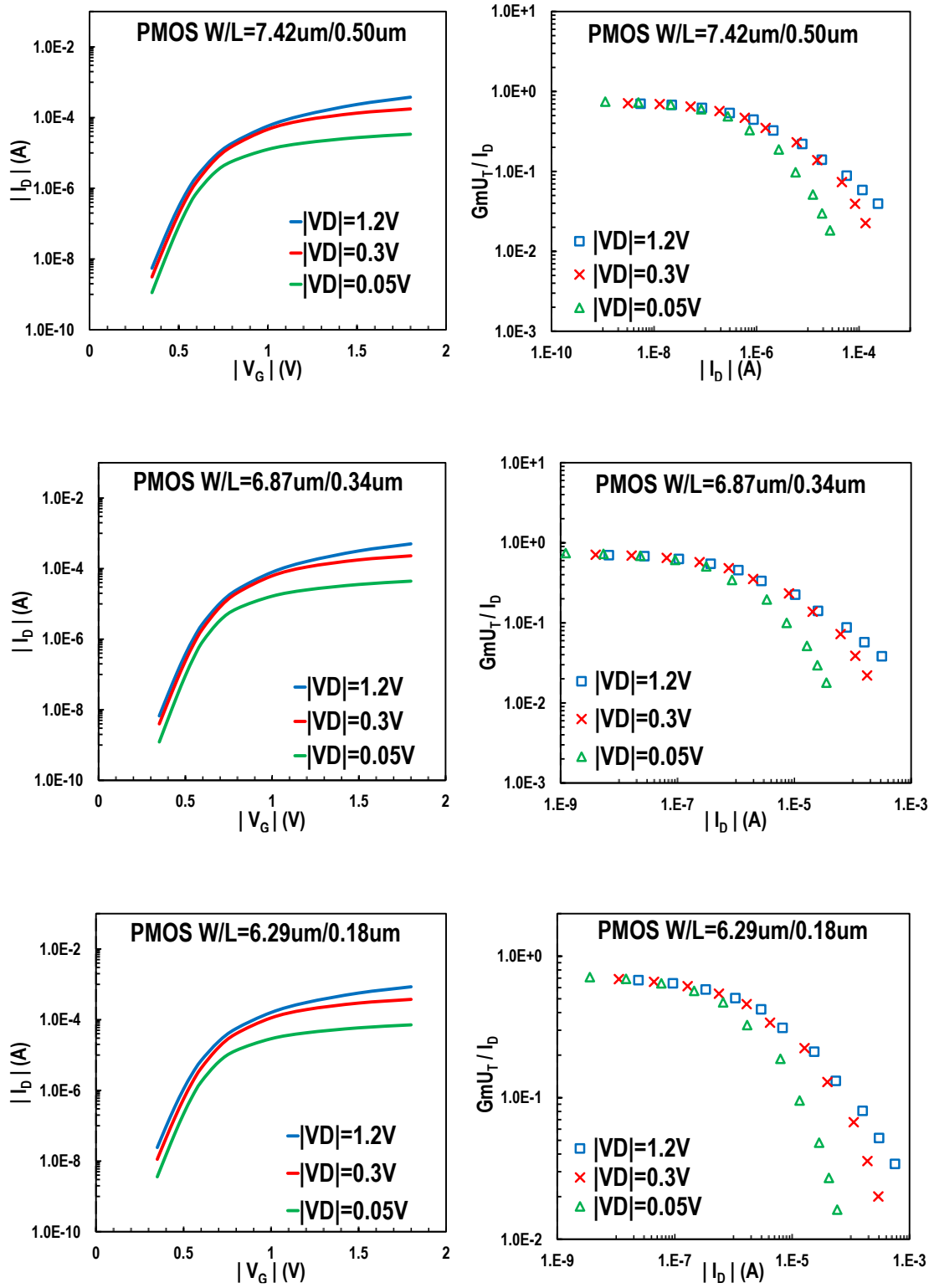
## 4.2 Measured I/V characteristics and drain-referred current noise PSDs

In this section the measured  $I_D$  vs.  $V_G$  plots along with some indicative measured current noise PSDs, will be presented. The  $|I_D|$  for every gate voltage value, represents the mean value of the measured drain current ( $|I_D|$ ), on a number of 50 NMOSFETs and 30 PMOSFETs on the same gate voltage. The unitless quantity  $G_m U_T / I_D$  is also calculated from the average  $G_m$  value that extracted from measurements.



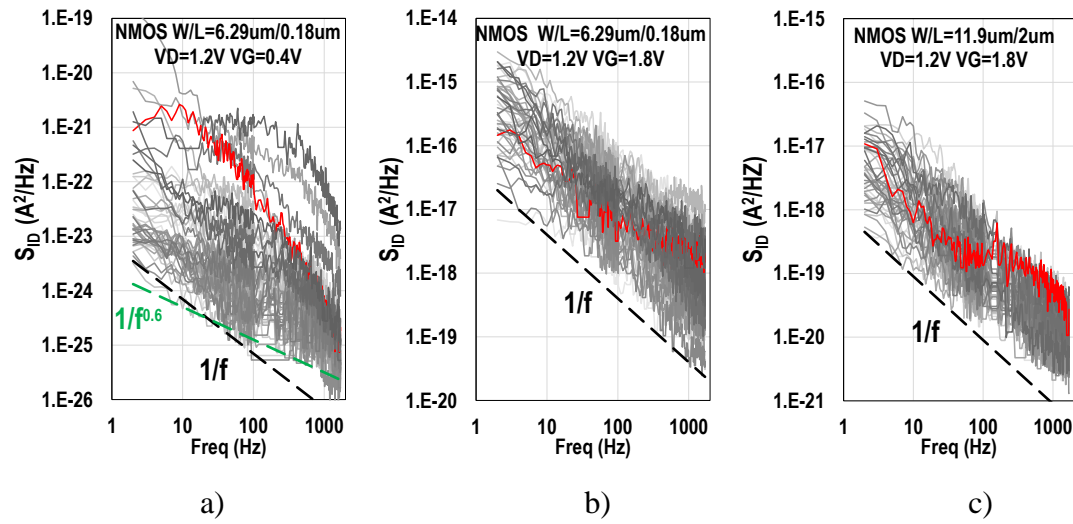
**Figure 4.4** Measured mean value of  $I_D$  (Log. Axis) vs  $V_G$  (left) and  $GmU_T/I_D$  vs.  $I_D$  (right), for 50 NMOSFETs with  $W/L=11.9\mu m/2\mu m$  and  $W/L=6.29\mu m/0.18\mu m$ , from weak to strong inversion ( $V_{GS} = 0.35, 0.45, 0.5, 0.55, 0.6, 0.65, 0.7, 0.8, 1.0, 1.2, 1.5$  and  $1.8V$ ), for both linear and saturation regions.



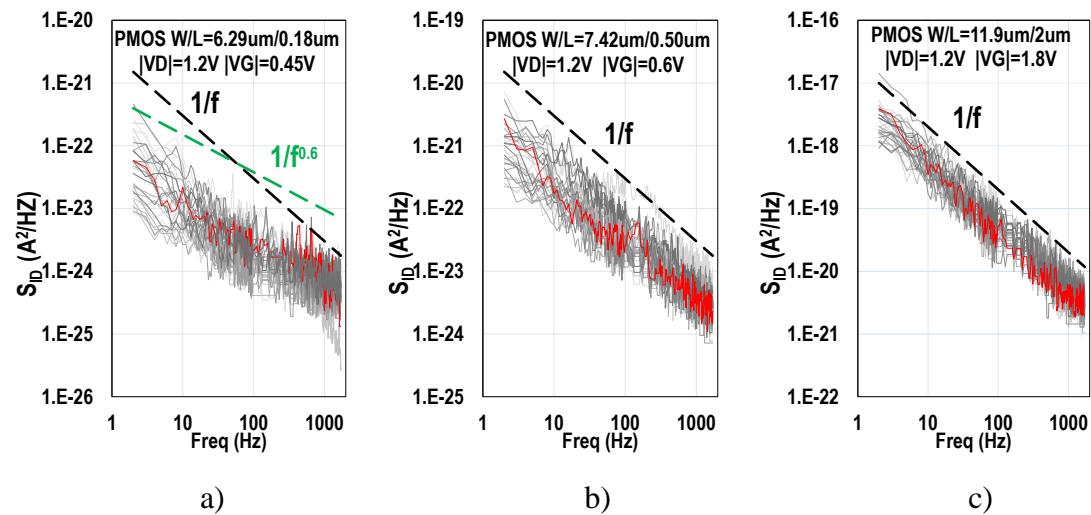


**Figure 4.5** Measured mean value of  $I_D$  (Log. Axis) vs  $V_G$  (left) and  $GmU_T/I_D$  vs.  $I_D$  (right), for 30 PMOSFETs with  $W/L=11.9\mu m/2\mu m$ ,  $7.42\mu m/0.5\mu m$ ,  $6.87\mu m/0.34$  and  $W/L=6.29\mu m/0.18\mu m$ , from weak to strong inversion ( $V_{GS} = 0.35, 0.45, 0.5, 0.55, 0.6, 0.65, 0.7, 0.8, 1.0, 1.2, 1.5$  and  $1.8V$ ), for both linear and saturation regions.

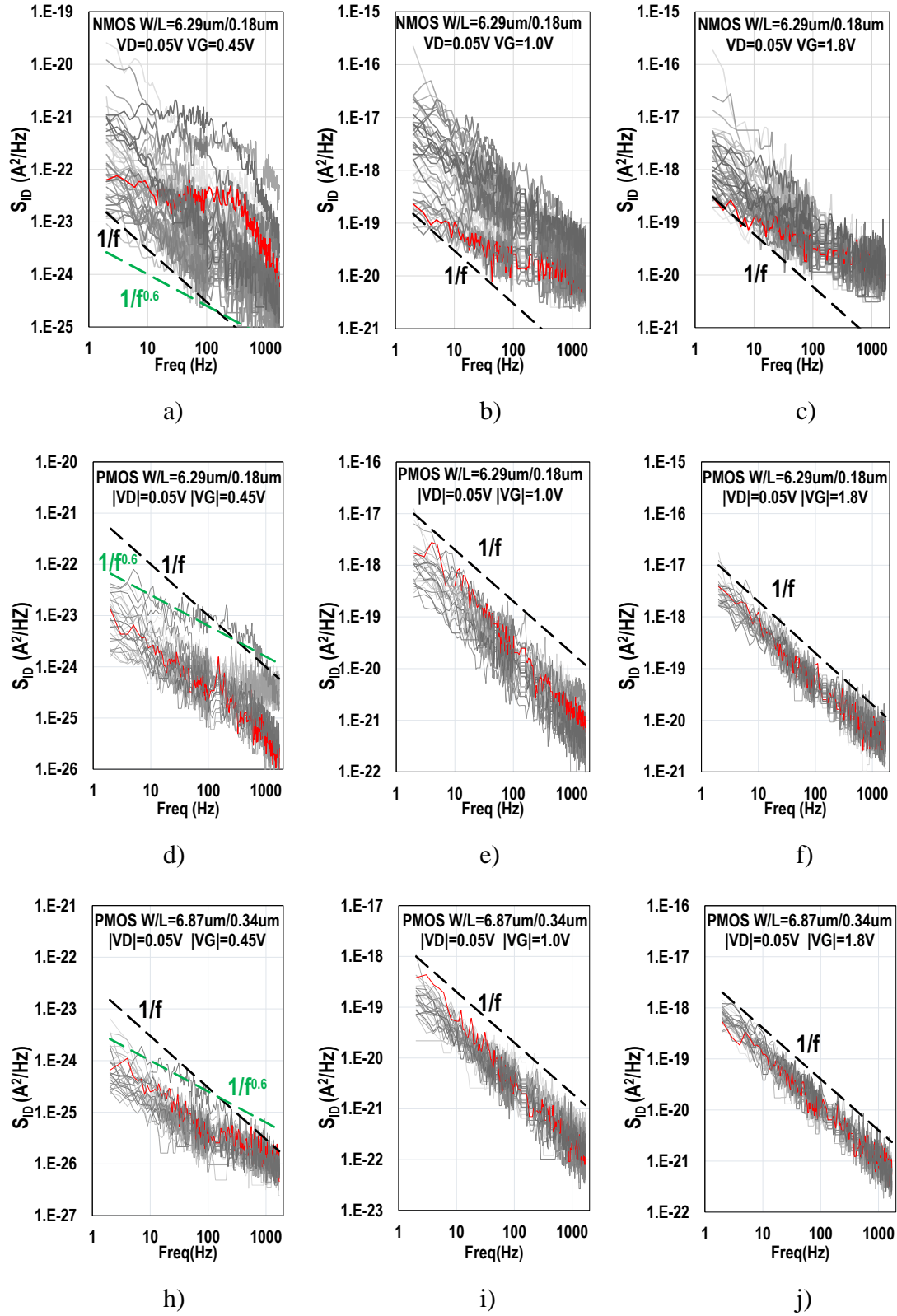
In Figures 4.6, 4.7 and 4.8 some indicative plots of the measured drain current noise PSDs are illustrated. The  $1/f$  trend line is also depicted. The PSD colored in red, represents how the noise spectral is formed over the same die for different bias conditions. We can observe that the noise dispersion is larger for smaller devices and lower gate voltages. Furthermore, NMOS devices show a higher noise variability than PMOS devices. For low gate voltages, the deviation of low frequency noise of the ideal  $1/f$  slope is clear. Also, the forming of a Lorentzian like PSD can be noticed in Figure 4.8 a).



**Figure 4.6** Measured relative power spectral density of drain current noise  $S_{ID}$  for 50 different N-channel MOSFETs with a)  $W/L=6.29\mu\text{m}/0.18\mu\text{m}$  and b,c)  $W/L=11.9\mu\text{m}/2\mu\text{m}$  at  $V_D=1.2\text{V}$  for a)  $V_G=0.4\text{V}$  and b,c)  $V_G=1.8\text{V}$ .



**Figure 4.7** Measured relative power spectral density of drain current noise  $S_{ID}$  for 30 different P-channel MOSFETs with a)  $W/L=6.29\mu\text{m}/0.18\mu\text{m}$ , b)  $W/L=11.9\mu\text{m}/2\mu\text{m}$  and c)  $W/L=7.42\mu\text{m}/0.5\mu\text{m}$  at  $|V_D|=1.2\text{V}$ , for a)  $|V_G|=0.45\text{V}$ , b)  $|V_G|=0.6\text{V}$  and c)  $|V_G|=1.8\text{V}$ .

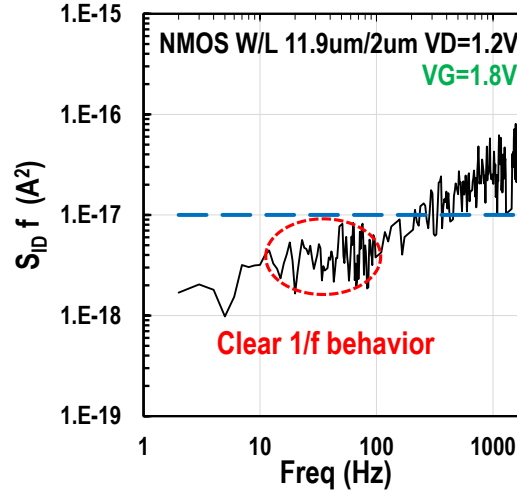


**Figure 4.8** Measured relative power spectral density of drain current noise  $S_{ID}$  for 50 different NMOSFETs with  $W/L=6.29\mu\text{m}/0.18\mu\text{m}$  (first row) and 30 different PMOSFETs with  $W/L=6.29\mu\text{m}/0.18\mu\text{m}$  (middle row) and  $W/L=6.87\mu\text{m}/0.34\mu\text{m}$  (last row), at linear region ( $|V_D|=0.05\text{V}$ ) for  $|V_G|=0.45\text{V}$ ,  $1.0\text{V}$  and  $1.8\text{V}$ .

### 4.3 Measured data processing and results

In this section, the measured data processing along with the extracted results will be demonstrated. For both PMOS and NMOS devices, the PSD of the  $1/f$  noise will be presented in the form of  $WLS_{IDf}/I_D^2$  ( $m^2$ ),  $WLS_{VGf}$  ( $V^2m^2$ ) versus  $I_D/(W/L)$  (A) and  $S_{IDf}$  ( $A^2$ ),  $S_{VGf}$  ( $V^2$ ) versus  $I_D$  (A) plots, whereas the  $1/f$  noise variability with  $\sigma(\ln(WLS_{ID}/I_D^2))$  versus  $I_D/(W/L)$  and  $1/\sqrt{WL}$  plots.

The measured data processing procedure is described as follows. The first step was to multiply every  $S_{ID}$  measured value with  $f$ . Then, the average  $S_{IDf}$  ( $A^2$ ) value was extracted from the frequency range between 10 and 30 Hz, where the clear  $1/f$  behavior can be observed for almost every bias condition and device (Figure 4.9). At



**Figure 4.9** Measured noise  $S_{IDf}$  vs. frequency for an NMOSFET with  $W=11.9\mu m$  and  $L=2\mu m$  at saturation region ( $V_D=1.2V$ ) for  $V_G=1.8V$ .

last, the quantity  $WLS_{IDf}/I_D^2$  was formed for every gate bias condition, where  $WL$  is the device area ( $\mu m^2$ ) and  $I_D$  is the measured drain current. The quantities  $WLS_{VGf}$  and  $S_{VGf}$  were calculated from the following equations:

$$WLS_{VGf} = (WLS_{IDf}) / G_m^2 \quad (4.1)$$

$$S_{VGf} = (S_{IDf}) / G_m^2 \quad (4.2)$$

and are expressed in  $V^2m^2$  and  $V^2$  respectively.  $G_m$  is the measured value of the gate transconductance.

The ln-mean value ( $\mu$ ), standard deviation ( $\sigma$ ) and standard error of the mean (SEM) of  $WLS_{IDf}/I_D^2$  were also extracted, for every gate bias condition, on a

population of 50 different NMOS and 30 different PMOS devices. First the quantity  $\ln(WLS_{IDf}/I_D^2)$  was calculated for every different sample. Then the average of all natural logs along with the standard deviation and the  $\pm 2$ -sigma deviation, where extracted. The entire procedure for 1 gate voltage bias condition is described in detail by the following equations:

$$\mu = e [ \ln (WLS_{IDf}/I_D^2)_{N / \#N} ] \quad , N=1.. \#N \quad (4.3)$$

$$\sigma = \sigma [ \ln (WLS_{IDf}/I_D^2)_{N} ] \quad , N=1.. \#N \quad (4.4)$$

$$\mu \pm 2\sigma = \mu \cdot e^{\pm 2\sigma} \quad (4.5)$$

$$SEM = \sigma / \sqrt{\#N} \quad (4.6)$$

$$\mu \pm SEM = \mu \cdot e^{\pm SEM} \quad (4.7)$$

where  $\#N$  is the number of different devices (30 for PMOS and 50 for NMOS).

The used model in order to simulate  $WLS_{IDf}/I_D^2$ ,  $WLS_{VGf}$ ,  $S_{IDf}$  and  $S_{VGf}$  quantities, in all levels of inversion for both linear and saturation mode, is the carrier number fluctuation with correlated mobility fluctuations model which is described by equations 3.11 and 3.12. The statistical behavior of  $1/f$  noise was modeled by the low frequency noise variability model that presented in section 3.4 and can be described by the following equation:

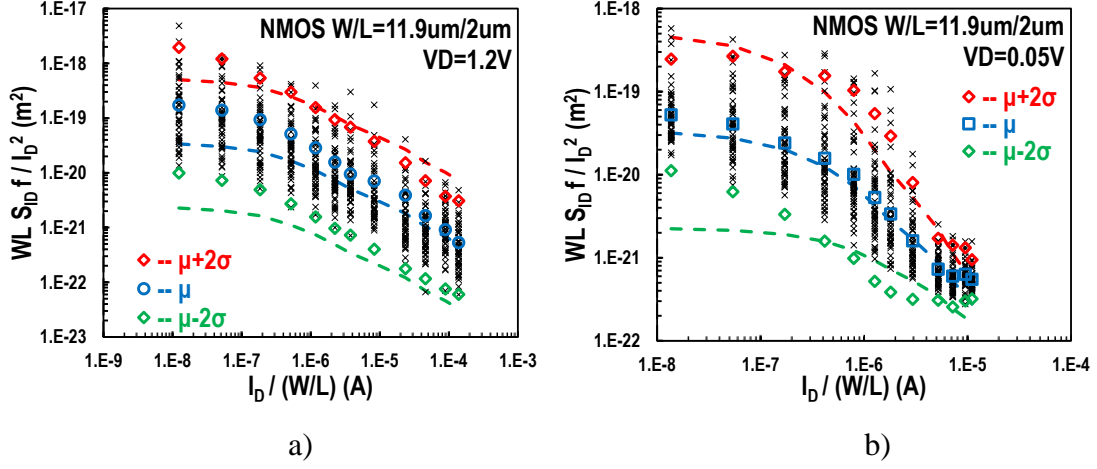
$$\sigma \left[ \ln \left( WL \cdot \frac{S_{ID}}{I_D^2} \cdot f \right) \right] = \sqrt{B^2 \frac{gmU_T}{I_D} + \frac{A^2}{WL}} \quad (4.8)$$

Through formulas 3.11, 3.12 and 4.8 a single set of parameters  $N_t$ ,  $\alpha c$ ,  $A$  and  $B$  was extracted and used for each type of transistors (NMOSFETs and PMOSFETs), for all geometries and bias conditions. The results are presented in Table 4.2, at the end of this section.

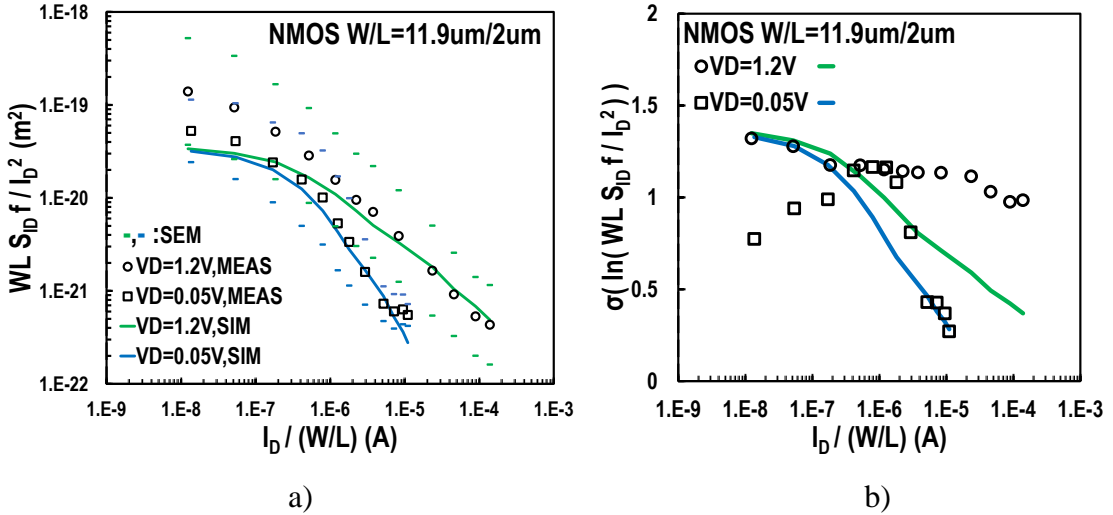
In sections 4.3.1 and 4.3.2 a list of figures containing measured and simulated curves, for both NMOS and PMOS devices, will be demonstrated. The results will be presented in both cases in the form of  $WLS_{IDf}/I_D^2$  and  $WLS_{VGf}$  versus  $|I_D|/(W/L)$ ,  $S_{IDf}$  and  $S_{VGf}$  versus  $|I_D|$ , and  $\sigma(\ln(WLS_{IDf}/I_D^2))$  versus  $|I_D|/(W/L)$  and  $1/\sqrt{WL}$  plots, for all the different geometries (PMOSFETs:  $W/L=11.9\mu m/2\mu m$ ,  $7.42\mu m/0.5\mu m$ ,  $6.87\mu m/0.34\mu m$  and  $6.29\mu m/0.18\mu m$ , NMOSFETs:  $W/L=11.9\mu m/2\mu m$ , and  $6.29\mu m/0.18\mu m$ ) and for all the different bias conditions.



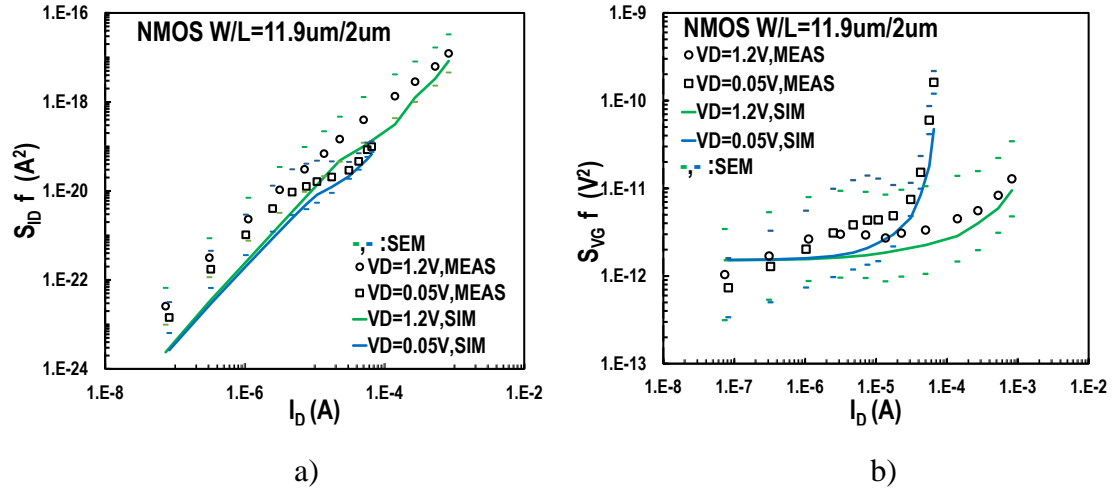
### 4.3.1 Results for enclosed gate NMOSFETs



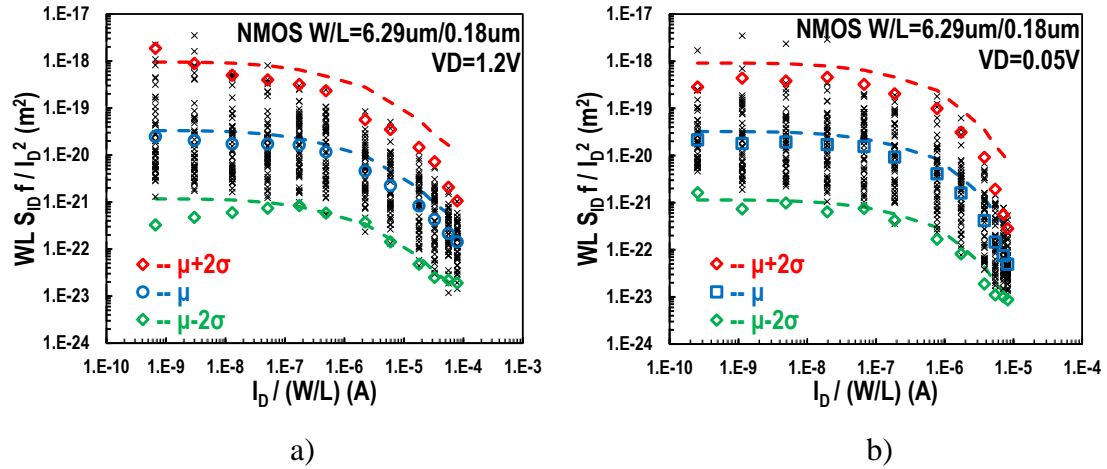
**Figure 4.10** Low frequency noise PSD  $S_{ID}/I_D^2$  multiplied with device area (WL) referred to 1 Hz measured at a)  $V_D=1.2\text{V}$  and b)  $V_D=0.05\text{V}$  versus normalized drain current  $I_D/(W/L)$ , for NMOS transistors with  $W/L=11.9\mu\text{m}/2\mu\text{m}$ . Measured noise: crosses. Measured average noise,  $\pm 2$ -sigma deviation: open markers. Model: average noise,  $\pm 2$ -sigma deviation: dashed lines.



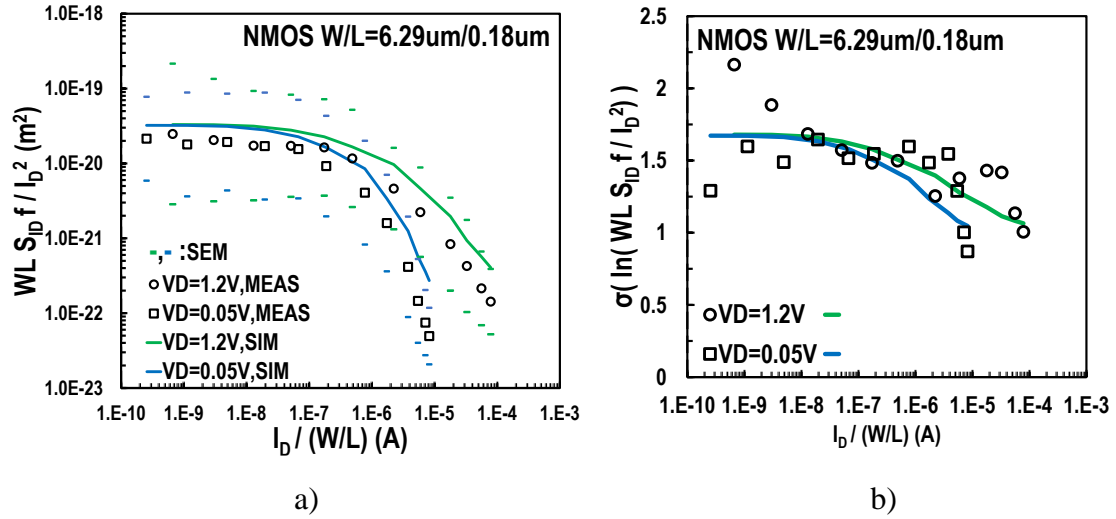
**Figure 4.11** a) Mean value of  $WLS_{ID}f/I_D^2$  versus  $I_D/(W/L)$  for NMOS transistors with  $W/L=11.9\mu\text{m}/2\mu\text{m}$ , from weak to strong inversion for both  $V_D=1.2\text{V}$  and  $0.05\text{V}$ . Measurements: markers. Model: lines. Standard error of the mean (SEM) is also depicted. b) Normalized standard deviation of the natural logarithm of  $1/f$  noise  $\sigma(\ln(WLS_{ID}f/I_D^2))$  versus normalized drain current  $I_D/(W/L)$ , for the same transistors and bias conditions. Measurements: markers. Model: lines.



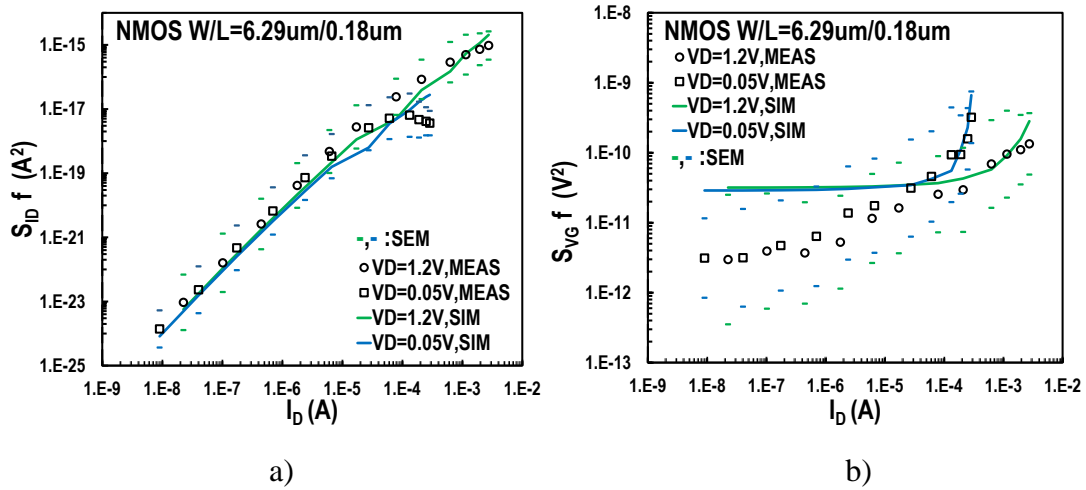
**Figure 4.12** PSD of 1/f noise at 1Hz a) in drain current  $S_{ID}f$  and b) in gate voltage  $S_{VG}f$  versus drain current  $I_D$ , for NMOS devices with  $W/L=11.9\mu\text{m}/2\mu\text{m}$  from weak to strong inversion for both linear ( $V_D=0.05\text{V}$ ) and saturation ( $V_D=1.2\text{V}$ ) regions. Measurements: markers. Model: lines. Standard error of the mean (SEM) is also depicted.



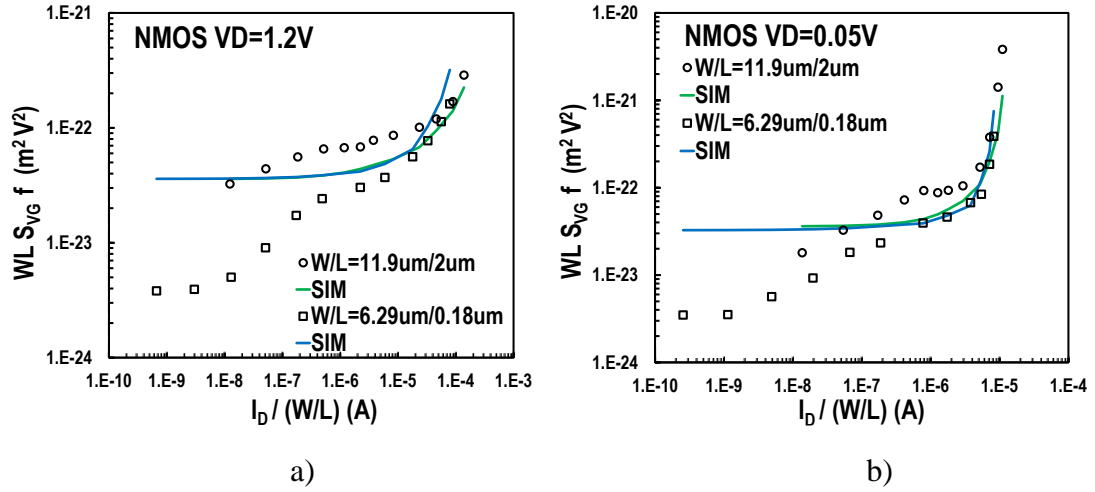
**Figure 4.13** Low frequency noise PSD  $S_{ID}/I_D^2$  multiplied with device area (WL), referred to 1 Hz measured at a)  $V_D=1.2\text{V}$  and b)  $V_D=0.05\text{V}$  versus normalized drain current  $I_D/(W/L)$ , for NMOS transistors with  $W/L=6.29\mu\text{m}/0.18\mu\text{m}$ . Measured noise: crosses. Measured average noise,  $\pm 2$ -sigma deviation: open markers. Model: average noise,  $\pm 2$ -sigma deviation: dashed lines.



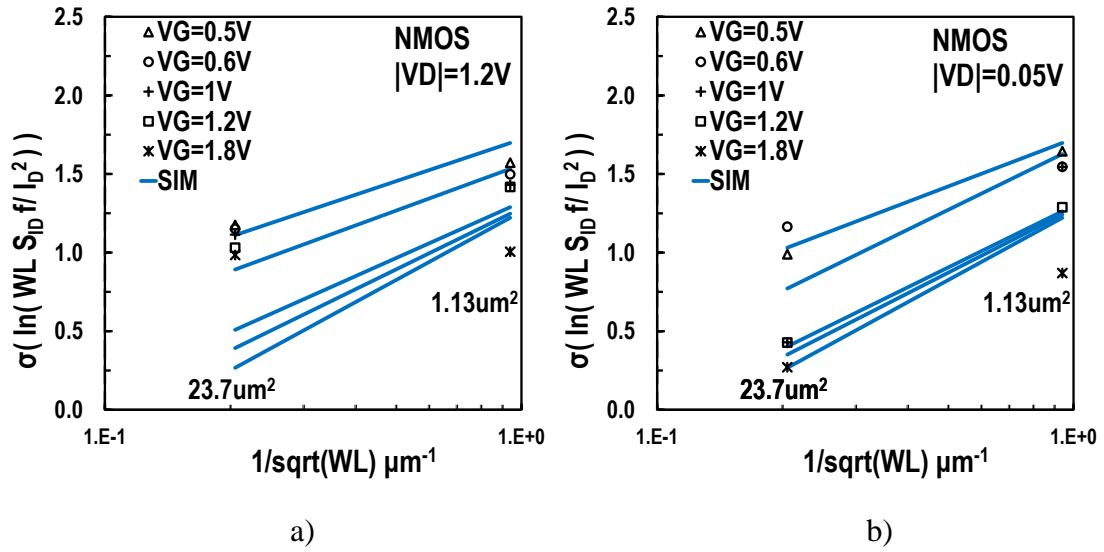
**Figure 4.14** a) Mean value of  $WLS_{ID}f/I_D^2$  versus  $I_D/(W/L)$  for NMOS transistors with  $W/L=11.9\mu m/2\mu m$ , from weak to strong inversion for both  $V_D=1.2V$  and  $0.05V$ . Measurements: markers. Model: lines. Standard error of the mean (SEM) is also depicted. b) Normalized standard deviation of the natural logarithm of  $1/f$  noise  $\sigma(\ln(WLS_{ID}f/I_D^2))$  versus normalized drain current  $I_D/(W/L)$ , for the same transistors and bias conditions. Measurements: markers. Model: lines.



**Figure 4.15** PSD of  $1/f$  noise at 1Hz a) in drain current  $S_{ID}f$  and b) in gate voltage  $S_{VG}f$  versus drain current  $I_D$ , for NMOS devices with  $W/L=6.29\mu m/0.18\mu m$  from weak to strong inversion for both linear ( $V_D=0.05V$ ) and saturation ( $V_D=1.2V$ ) regions. Measurements: markers. Model: lines. Standard error of the mean (SEM) is also depicted.

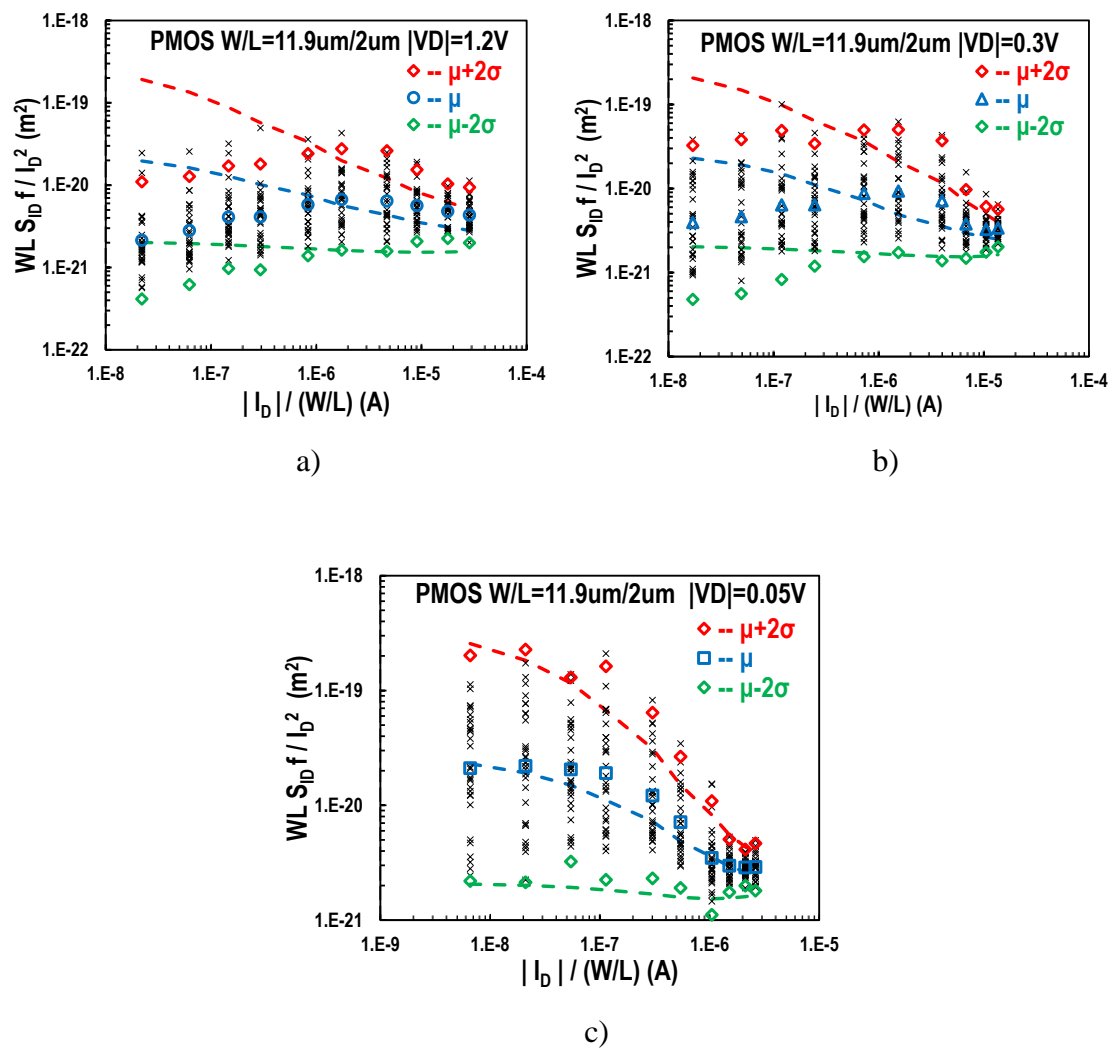


**Figure 4.16** PSD of 1/f noise at 1Hz in gate voltage normalized with area  $W L S_{VG} f$  versus normalized drain current  $I_D/(W/L)$ , for NMOS devices with  $W/L=11.9 \mu\text{m}/2 \mu\text{m}$  and  $W/L=6.29 \mu\text{m}/0.18 \mu\text{m}$  at a)  $V_D=1.2 \text{V}$  and b)  $V_D=0.05 \text{V}$  in all regions of inversion. Measurements: markers. Model: lines.

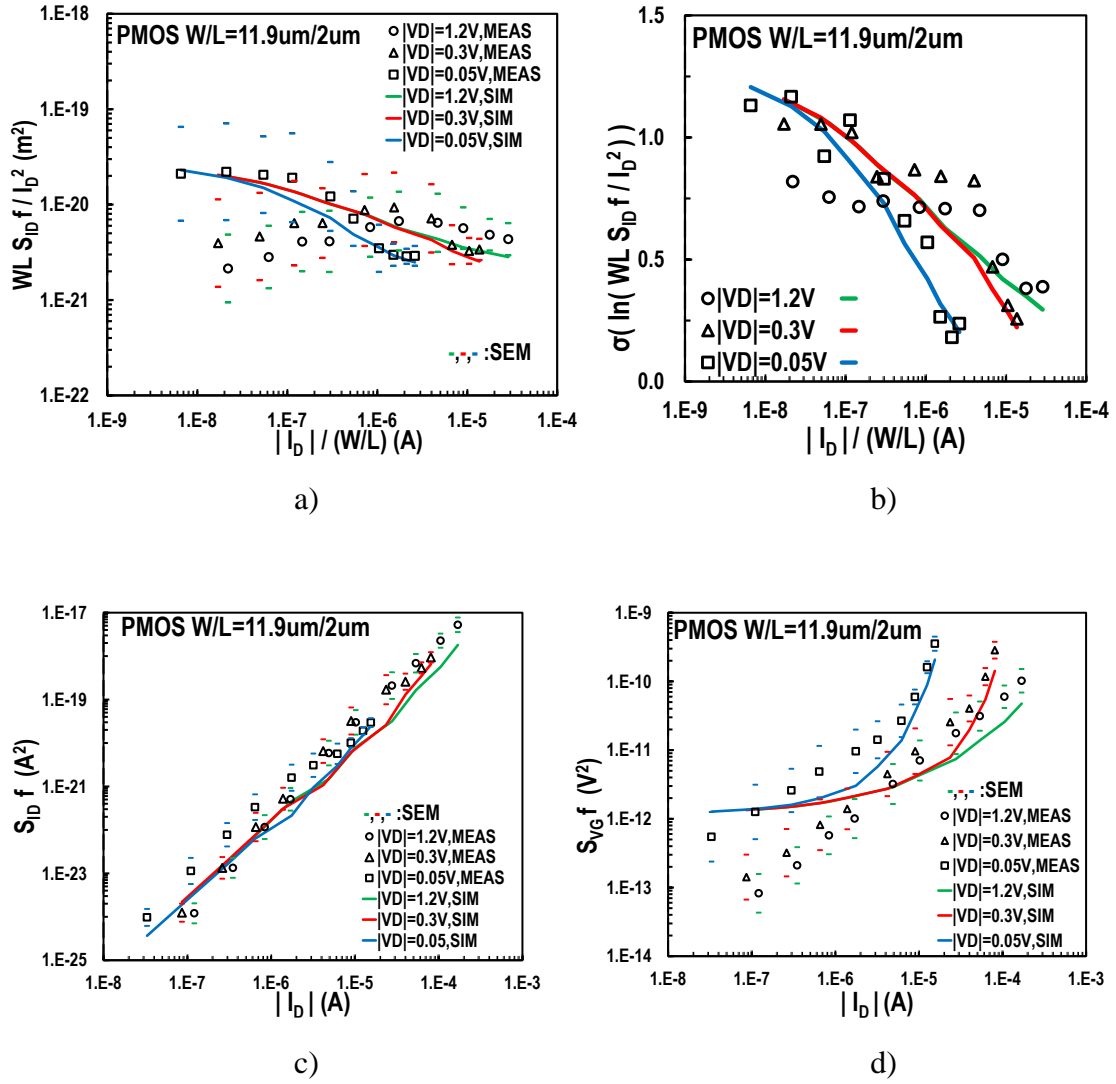


**Figure 4.17** Normalized standard deviation of the natural logarithm of 1/f noise  $\ln(W L S_{ID} f / I_D^2)$  referred to 1 Hz versus the inverse square root of the surface, for NMOS transistors at  $V_D=1.2$  and  $0.05 \text{V}$ . Measurements: markers, Model: lines.

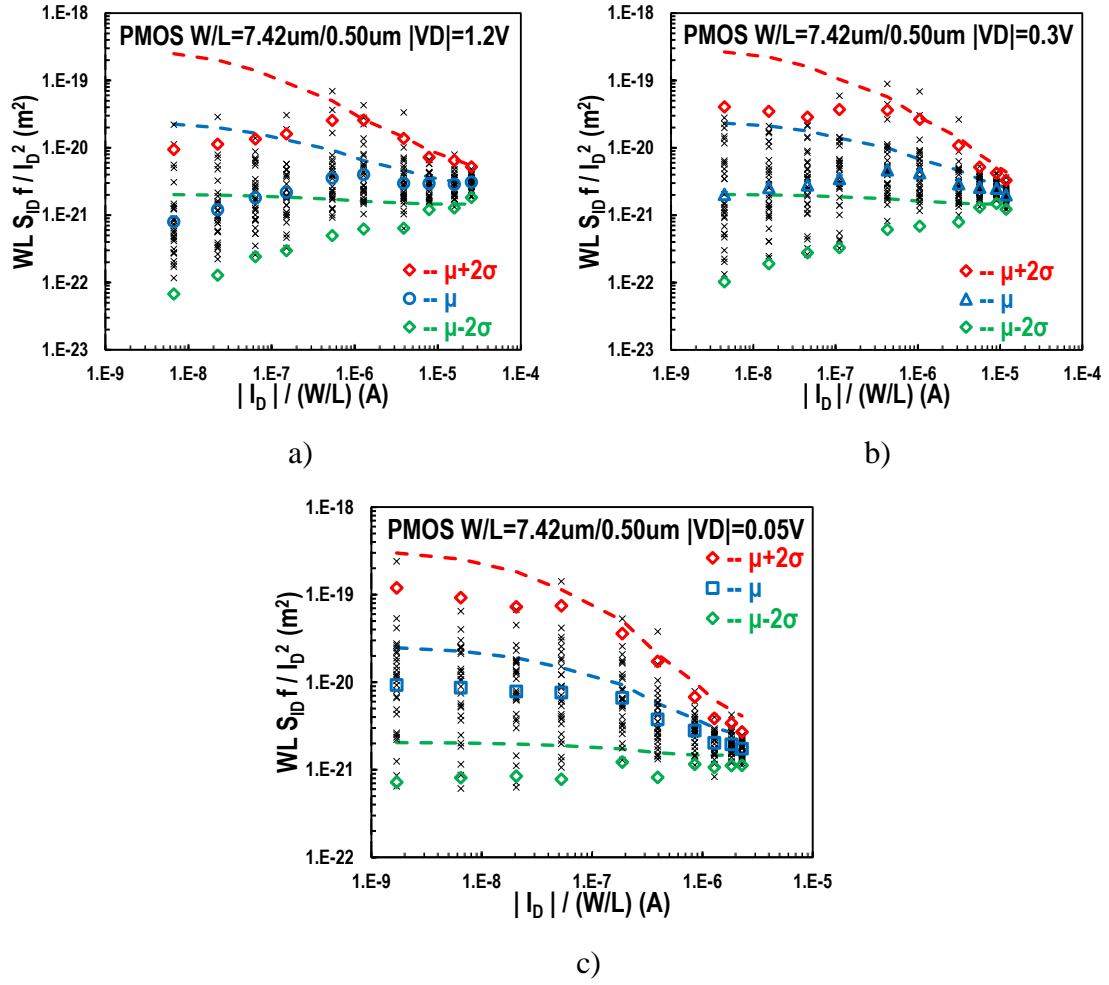
### 4.3.2 Results for enclosed gate PMOSFETs



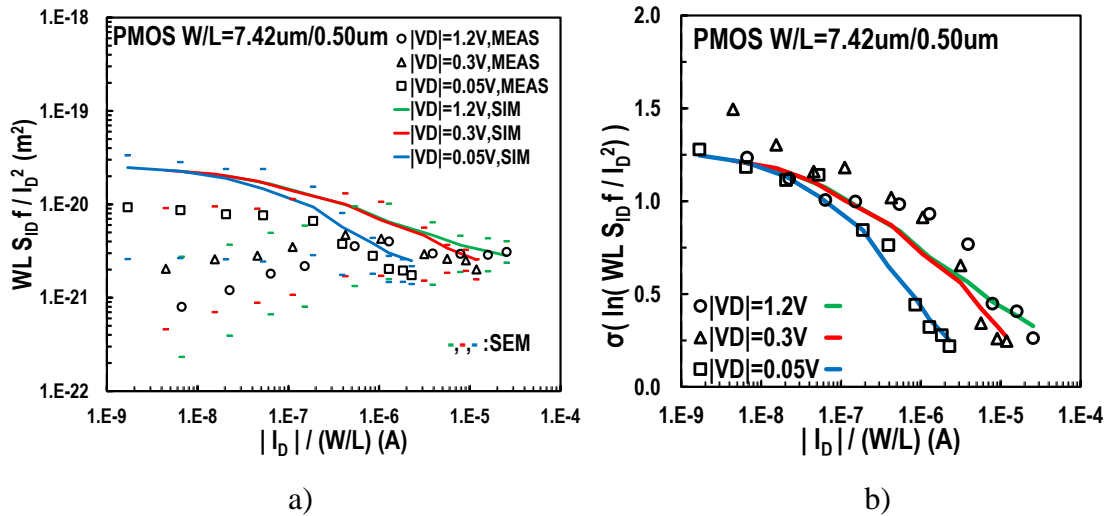
**Figure 4.18** Low frequency noise PSD  $S_{ID}/I_D^2$  multiplied with device area (WL) referred to 1 Hz measured at  $|V_D|=1.2\text{V}$ ,  $0.3\text{V}$  and  $0.05\text{V}$  versus normalized drain current  $|I_D|/(W/L)$ , for PMOS transistors with  $W/L=11.9\mu\text{m}/2\mu\text{m}$ . Measured noise: crosses. Measured average noise,  $\pm 2$ -sigma deviation: open markers. Model: average noise,  $\pm 2$ -sigma deviation: dashed lines.

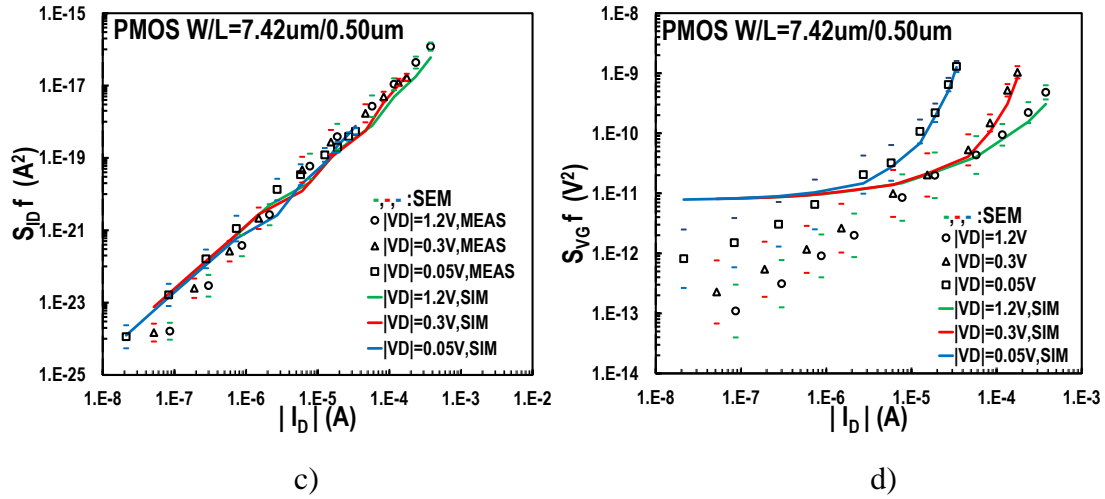


**Figure 4.19** a) Mean value of  $WLS_{IDf}/I_D^2$  versus  $|I_D|/(W/L)$ , c) PSD of  $1/f$  noise at  $1\text{Hz}$  in drain current  $S_{IDf}$  and d) in gate voltage  $S_{VGf}$  versus drain current  $|I_D|$  for PMOS transistors with  $W/L=11.9\mu\text{m}/2\mu\text{m}$ , from weak to strong inversion at  $|V_D|=1.2\text{V}$ ,  $0.3\text{V}$  and  $0.05\text{V}$ . Measurements: markers. Model: lines. Standard error of the mean (SEM) is also depicted. b) Normalized standard deviation of the natural logarithm of  $1/f$  noise  $\sigma(\ln(WLS_{IDf}/I_D^2))$  versus normalized drain current  $|I_D|/(W/L)$ , for the same transistors and bias conditions. Measurements: markers. Model: lines.

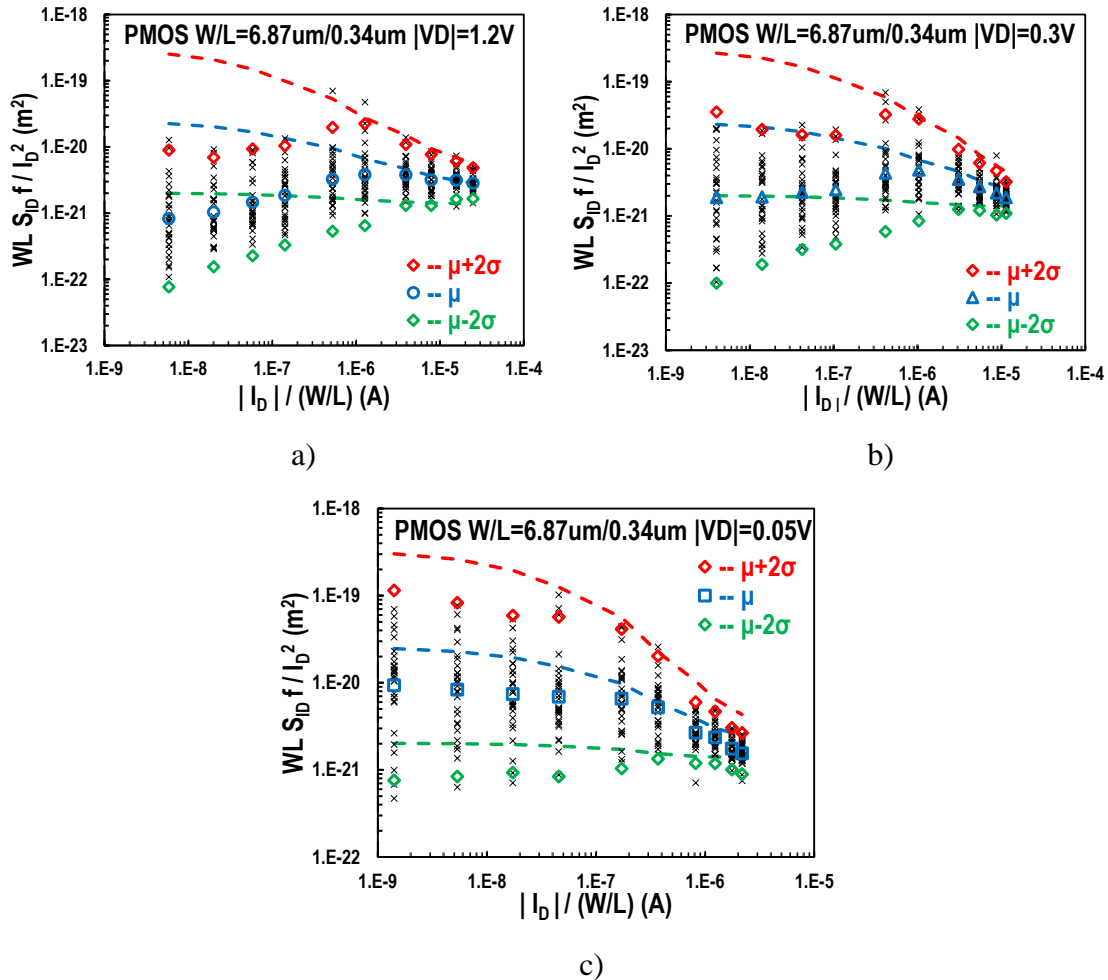


**Figure 4.20** Low frequency noise PSD  $S_{ID}/I_D^2$  multiplied with device area (WL), referred to 1 Hz measured at  $|V_D|=1.2\text{V}$ ,  $0.3\text{V}$  and  $0.05\text{V}$  versus normalized drain current  $|I_D|/(W/L)$ , for PMOS transistors with  $W/L=7.42\mu\text{m}/0.50\mu\text{m}$ . Measured noise: crosses. Measured average noise,  $\pm 2$ -sigma deviation: open markers. Model: average noise,  $\pm 2$ -sigma deviation: dashed lines.



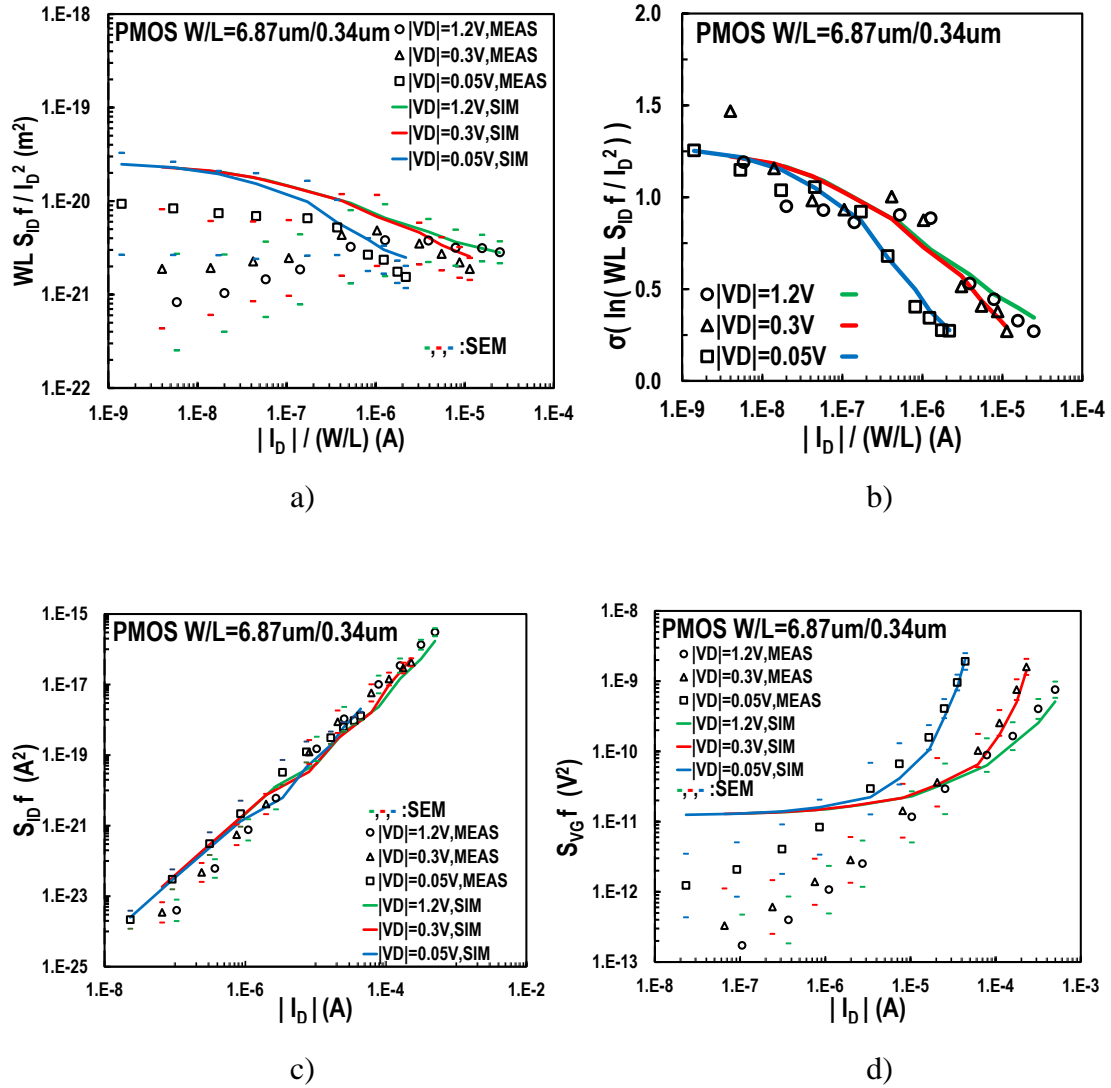


**Figure 4.21** a) Mean value of  $WLS_{ID}f/I_D^2$  versus  $|I_D|/(W/L)$ , c) PSD of 1/f noise at 1Hz in drain current  $S_{ID}f$  and d) in gate voltage  $S_{VG}f$  versus drain current  $|I_D|$  for PMOS transistors with  $W/L = 7.42\mu\text{m}/0.50\mu\text{m}$ , from weak to strong inversion at  $|V_D| = 1.2\text{V}$ ,  $0.3\text{V}$  and  $0.05\text{V}$ . Measurements: markers. Model: lines. Standard error of the mean (SEM) is also depicted. b) Normalized standard deviation of the natural logarithm of 1/f noise  $\sigma(\ln(WLS_{ID}f/I_D^2))$  versus normalized drain current  $|I_D|/(W/L)$ , for the same transistors and bias conditions. Measurements: markers. Model: lines.

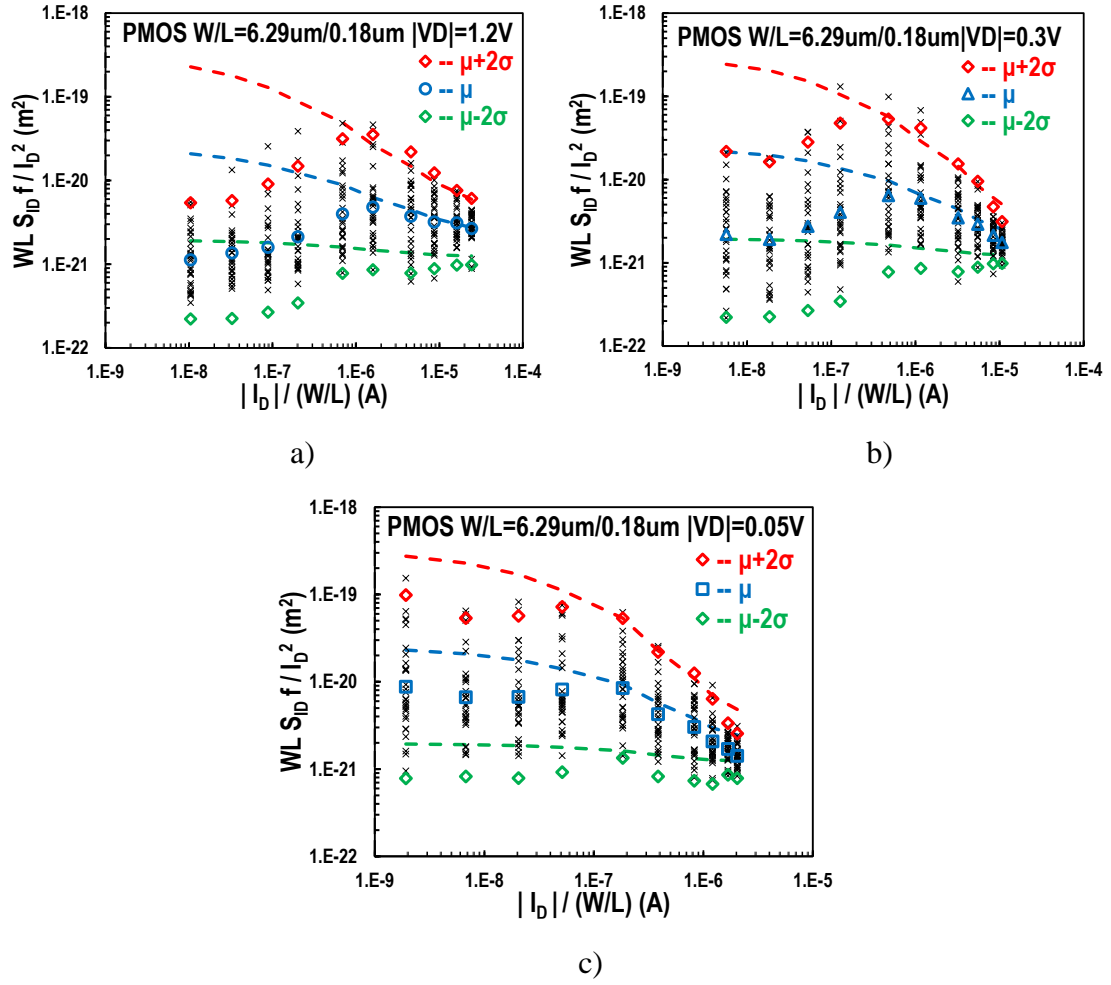




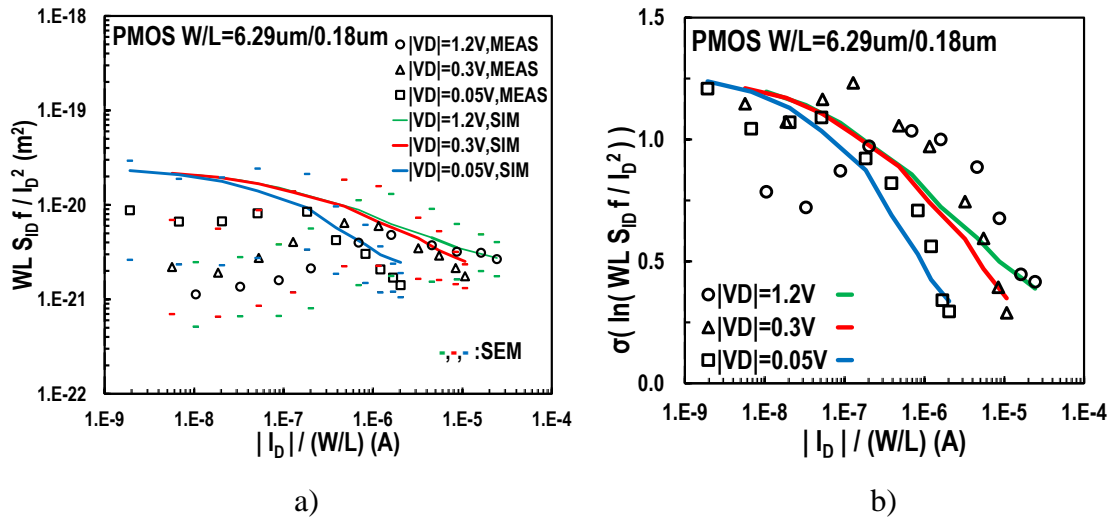
**Figure 4.22** Low frequency noise PSD  $S_{ID}/I_D^2$  multiplied with device area (WL), referred to 1 Hz measured Hz measured at  $|V_D|=1.2V$ ,  $0.3V$  and  $0.05V$  versus normalized drain current  $|I_D|/(W/L)$ , for PMOS transistors with  $W/L=6.87\mu m/0.34\mu m$ . Measured noise: crosses. Measured average noise,  $\pm 2$ -sigma deviation: open markers. Model: average noise,  $\pm 2$ -sigma deviation: dashed lines.

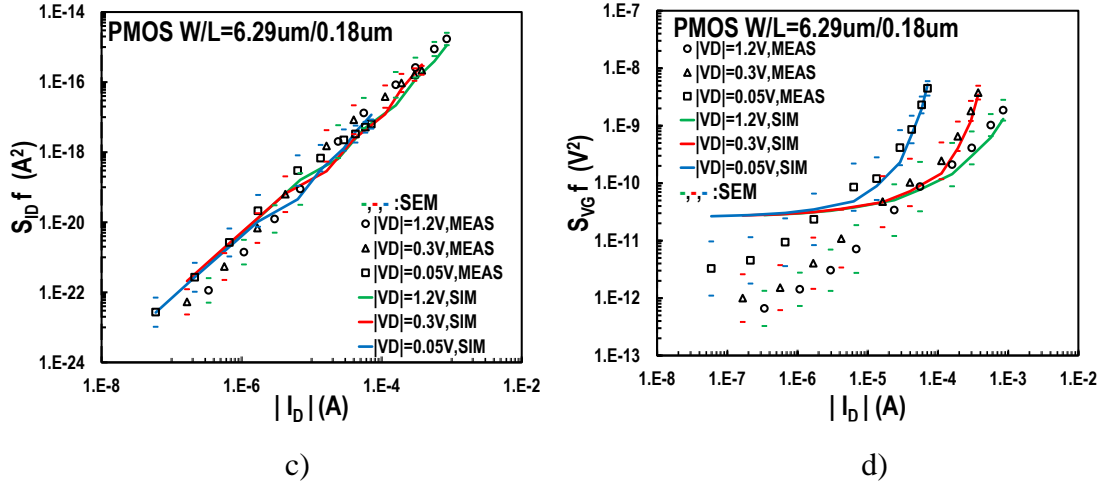


**Figure 4.23** a) Mean value of  $WLS_{IDf}/I_D^2$  versus  $|I_D|/(W/L)$ , c) PSD of  $1/f$  noise at 1Hz in drain current  $S_{IDf}$  and d) in gate voltage  $S_{VGf}$  versus drain current  $|I_D|$  for PMOS transistors with  $W/L=6.87\mu m/0.34\mu m$ , from weak to strong inversion at  $|V_D|=1.2V$ ,  $0.3V$  and  $0.05V$ . Measurements: markers. Model: lines. Standard error of the mean (SEM) is also depicted. b) Normalized standard deviation of the natural logarithm of  $1/f$  noise  $\sigma(\ln(WLS_{IDf}/I_D^2))$  versus normalized drain current  $|I_D|/(W/L)$ , for the same transistors and bias conditions. Measurements: markers. Model: lines.

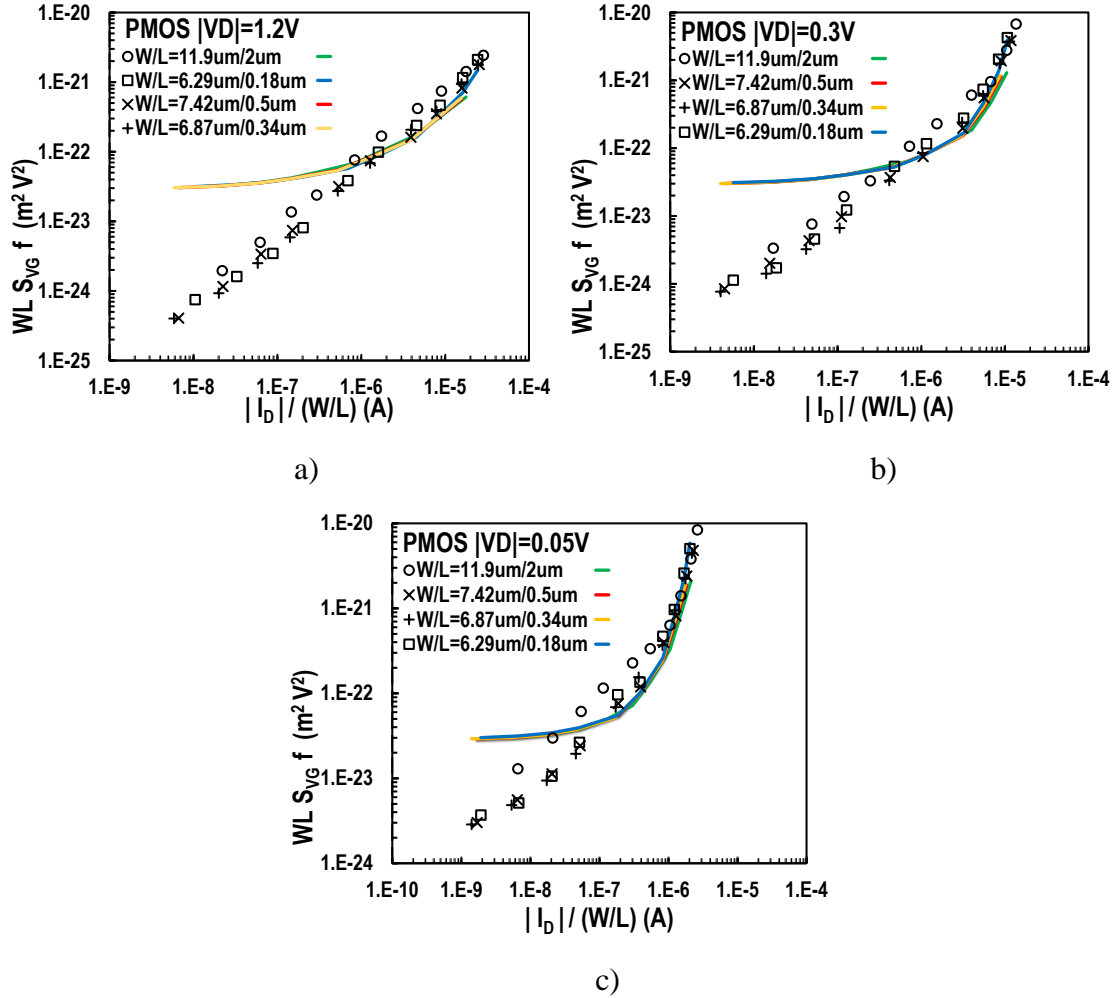


**Figure 4.24** Low frequency noise PSD  $S_{ID}/I_D^2$  multiplied with device area (WL), referred to 1 Hz measured at  $|V_D|=1.2\text{V}$ ,  $0.3\text{V}$  and  $0.05\text{V}$  versus normalized drain current  $|I_D|/(W/L)$ , for PMOS transistors with  $W/L=6.29\mu\text{m}/0.18\mu\text{m}$ . Measured noise: crosses. Measured average noise,  $\pm 2$ -sigma deviation: open markers. Model: average noise,  $\pm 2$ -sigma deviation: dashed lines.

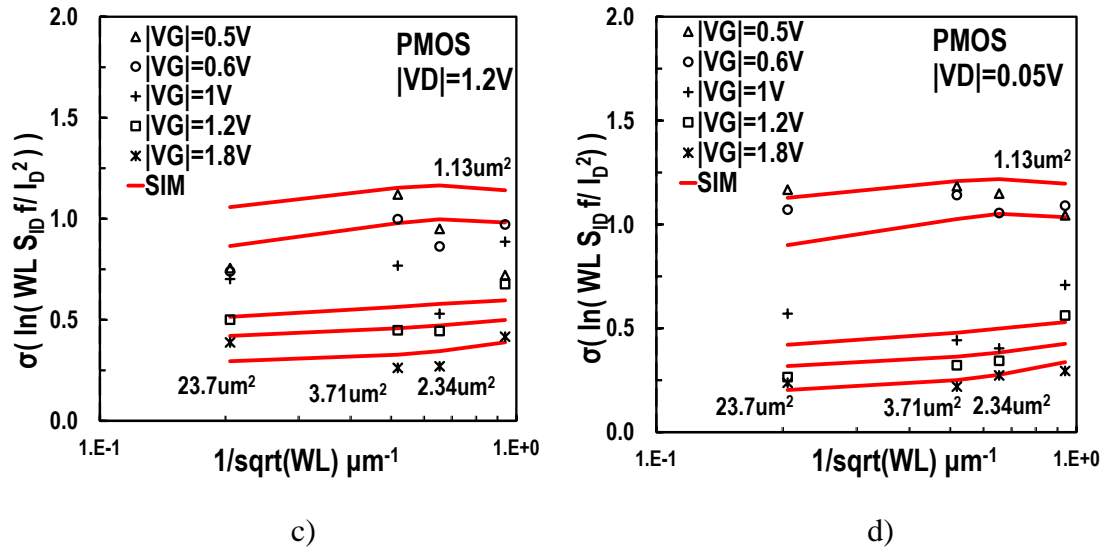




**Figure 4.25** a) Mean value of  $WLS_{ID}f/I_D^2$  versus  $|I_D|/(W/L)$ , c) PSD of 1/f noise at 1Hz in drain current  $S_{ID}f$  and d) in gate voltage  $S_{VG}f$  versus drain current  $|I_D|$  for PMOS transistors with  $W/L=6.29\mu\text{m}/0.18\mu\text{m}$ , from weak to strong inversion at  $|V_D|=1.2\text{V}$ ,  $0.3\text{V}$  and  $0.05\text{V}$ . Measurements: markers. Model: lines. Standard error of the mean (SEM) is also depicted. b) Normalized standard deviation of the natural logarithm of 1/f noise  $\sigma(\ln(WLS_{ID}f/I_D^2))$  versus normalized drain current  $|I_D|/(W/L)$ , for the same transistors and bias conditions. Measurements: markers. Model: lines.



**Figure 4.26** PSD of 1/f noise at 1Hz in gate voltage normalized with area  $WLS_{VGf}$  versus normalized drain current  $|I_D|/(W/L)$ , for PMOS devices with  $W/L=11.9\mu\text{m}/2\mu\text{m}$ ,  $7.42\mu\text{m}/0.5\mu\text{m}$ ,  $6.87\mu\text{m}/0.34\mu\text{m}$  and  $6.29\mu\text{m}/0.18\mu\text{m}$  at  $|V_D|=1.2\text{V}$ ,  $0.3\text{V}$  and  $0.05\text{V}$  in all regions of inversion. Measurements: markers. Model: lines.



**Figure 4.27** Normalized standard deviation of the natural logarithm of 1/f noise  $\ln(WLS_{IDf}/I_D^2)$ , referred to 1 Hz for PMOS devices, at  $|V_D|=1.2$  and  $0.05\text{V}$ , versus the inverse square root of the surface. Measurements: markers, Model: lines.

## 4.4 Extracted noise parameters and results validation

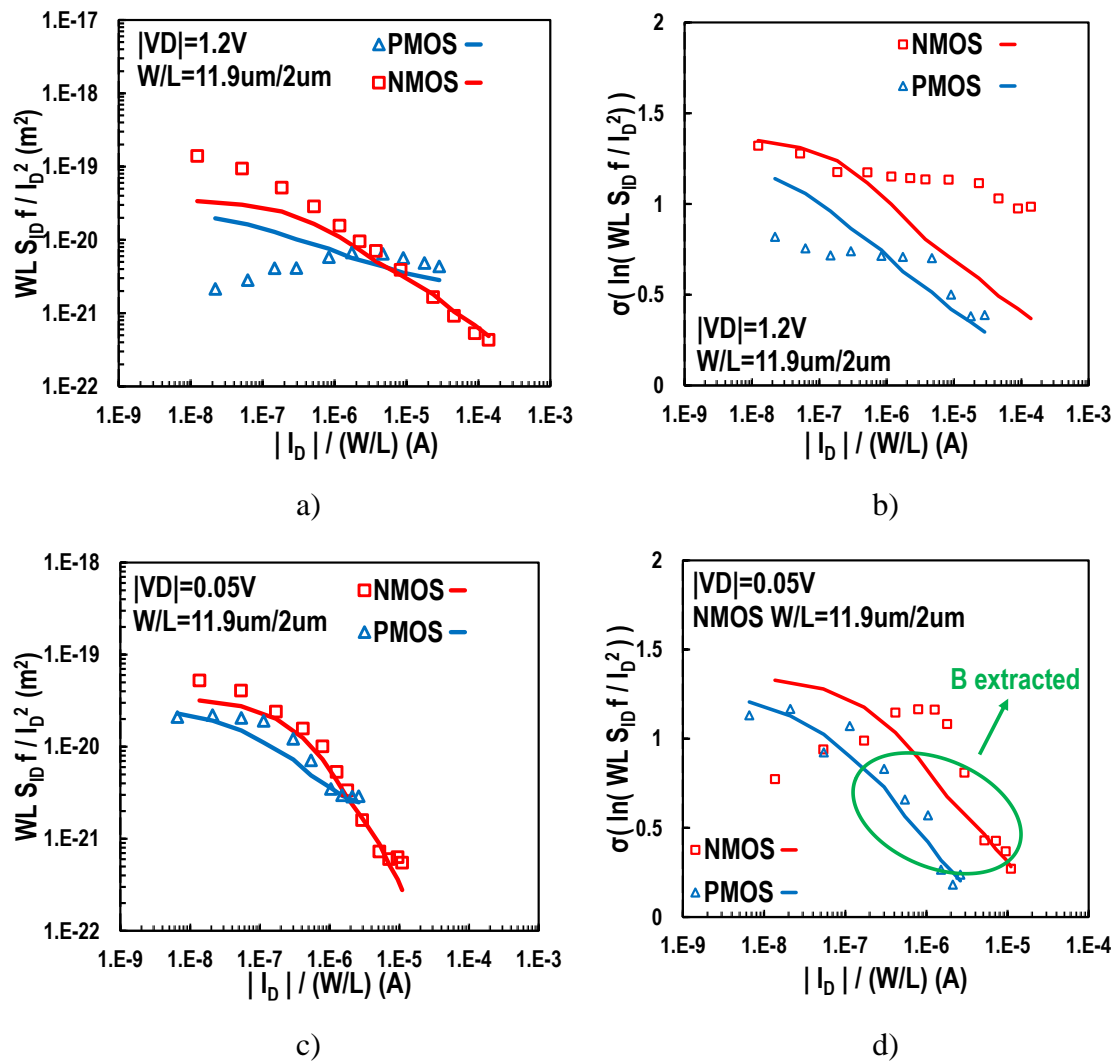
In table 4.2 the values of the parameters that used for calculations, in equations 3.11 and 3.12 are presented. Fitting parameters  $N_T$ ,  $\alpha_c$ , A and B that extracted from both carrier number fluctuation model (equations 3.11, 3.12) and 1/f variability model (equation 4.8), are listed in table 4.1. Parameter  $N_T$  was extracted on weak inversion from  $WLS_{IDf}/I_D^2$  quantity. The extracted values, was found close to the typical values for both kind of devices. Parameter  $\alpha_c$ , extracted from strong inversion and has a larger value for PMOSFETs as expected.

Parameter	Units	NMOS	PMOS
$N_T$	$\text{eV}^{-1}\text{cm}^{-3}$	$4.64 \cdot 10^{16}$	$2.16 \cdot 10^{16}$
$\alpha_c$	$\text{VsC}^{-1}$	$6.6 \cdot 10^3$	$2.15 \cdot 10^5$
A	$\mu\text{m}$	1.1	0.3
B	-	1.52	1.45

**Table 4.1** 1/f LFN noise parameters, extracted for enclosed gate MOSFETs, on a 0.18um CMOS technology.

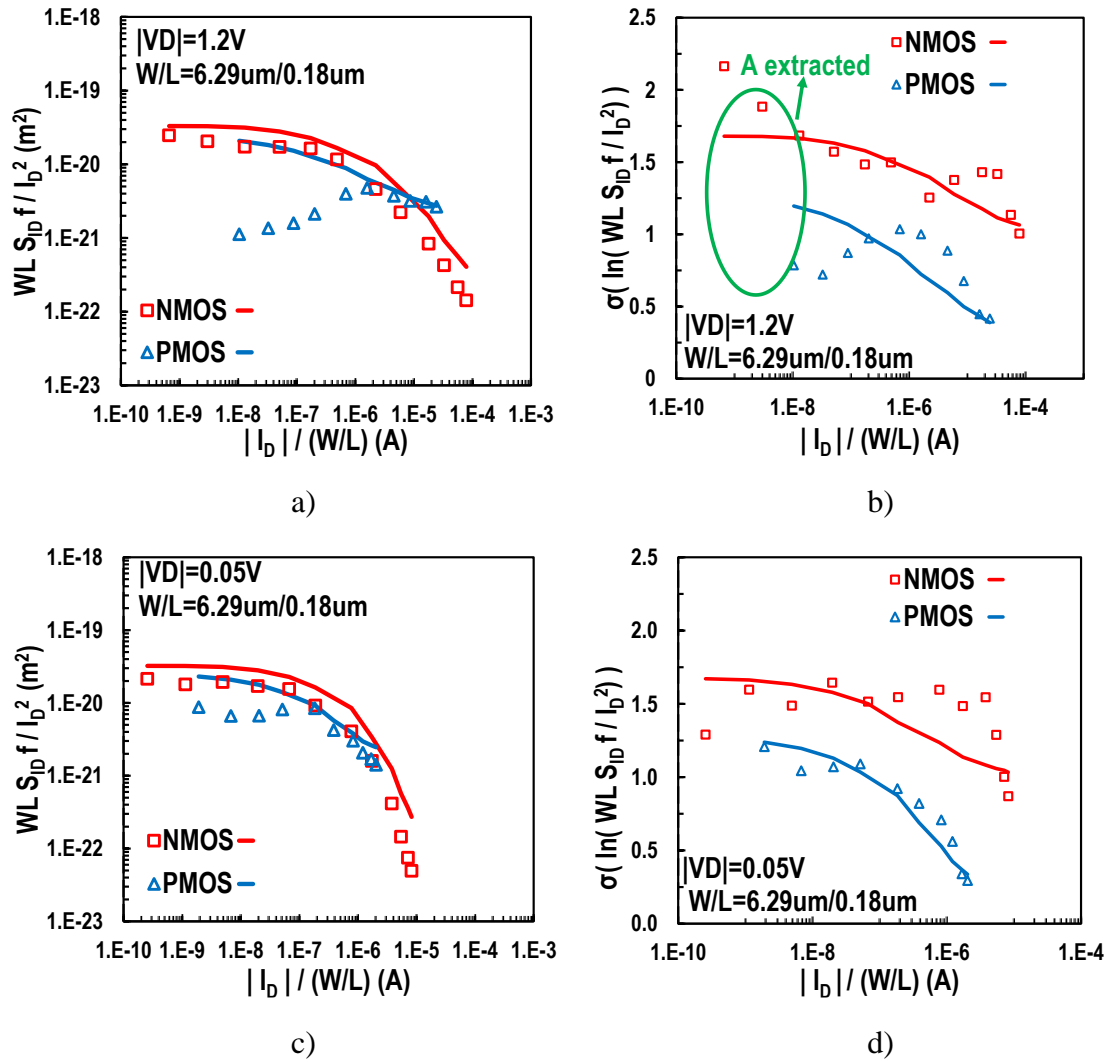
Parameter	Units	NMOS	PMOS
k	J/K	$1.308 \cdot 10^{-23}$	
T	K	300	
$\lambda$	nm	0.1	
q	C	$1.602 \cdot 10^{-19}$	
$U_T$	mV	25.8	
$C_{ox}$	F/m <sup>2</sup>	0.01	
$\mu$	cm <sup>2</sup> Vs <sup>-1</sup>	380	58

**Table 4.2** List of parameters that used for calculations in equations 3.11 and 3.12.



**Figure 4.28** a,c) Mean value of  $WLS_{ID}f/I_D^2$  versus  $|I_D|/(W/L)$ , for NMOS and PMOS devices with  $W/L=11.9\mu m/2\mu m$ , from weak to strong inversion at  $|V_D|=1.2V$  and

0.05V. b,d) Normalized standard deviation of the natural logarithm of 1/f noise  $\sigma(\ln(WL S_{ID} f / I_D^2))$  versus normalized drain current  $|I_D|/(W/L)$ , for the same transistors and bias conditions. Measurements: markers, Model: lines.



**Figure 4.29** a,c) Mean value of  $WLS_{ID}f/I_D^2$  versus  $|I_D|/(W/L)$ , for NMOS and PMOS devices with  $W/L=6.29\mu\text{m}/0.18\mu\text{m}$ , from weak to strong inversion at  $|V_D|=1.2\text{V}$  and  $0.05\text{V}$ . b,d) Normalized standard deviation of the natural logarithm of 1/f noise  $\sigma(\ln(WLS_{ID}f/I_D^2))$  versus normalized drain current  $|I_D|/(W/L)$ , for the same transistors and bias conditions. Measurements: markers, Model: lines.

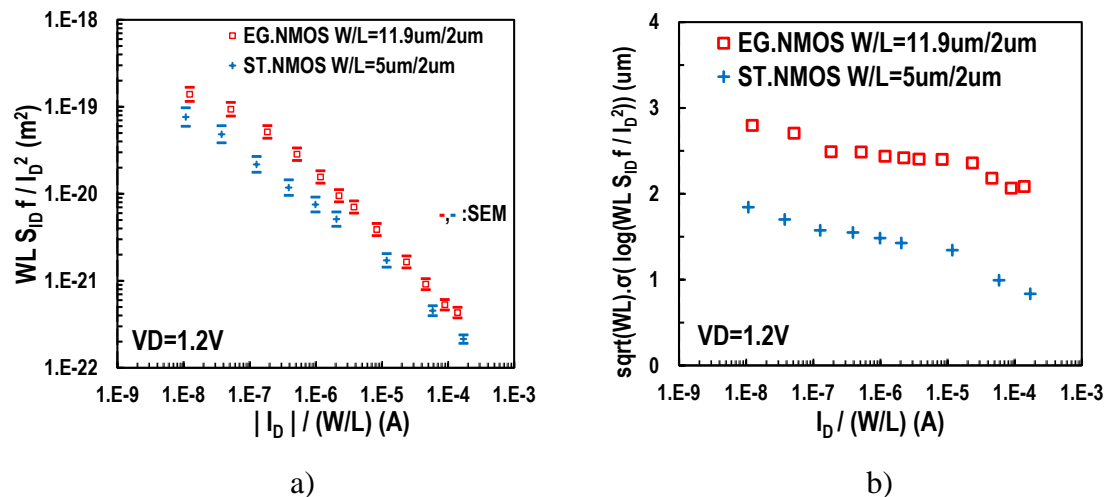
For both enclosed gate NMOSFETs and PMOSFETs, the basic carrier number fluctuation model describes adequately noise behavior. Short channel NMOS devices present lower noise against long channel NMOS devices, in weak inversion at a given drain current, for both linear and saturation region of operation. Furthermore, long channel NMOS transistors show some indication of mobility fluctuation. PMOS devices, in weak inversion, show a reduce noise level at increased drain voltage. This noise reduction is interestingly accompanied by noise variability reduction. The LFN noise variability model that used, gives overall very good results for the studied enclosed gate MOSFETs. NMOS devices show a higher variability than PMOS devices

but lower noise levels. This is similarly as in standard transistors. The area-related statistical parameter A was extracted from weak inversion, whereas the bias-related statistical parameter B from strong inversion. It can also be noticed that noise variability follows the  $gmU_T/I_D$  behavior as in standard transistors. The behavior of the simulated  $\pm 2$ -sigma deviation plots follows the dispersion of measurements, especially for NMOS transistors whereas in PMOS devices, the model presents better results for linear region of operation. The choice of  $\pm 2$ -sigma deviation values is not strict and the model can be used with larger spread e.g.  $\pm 3\sigma$ .

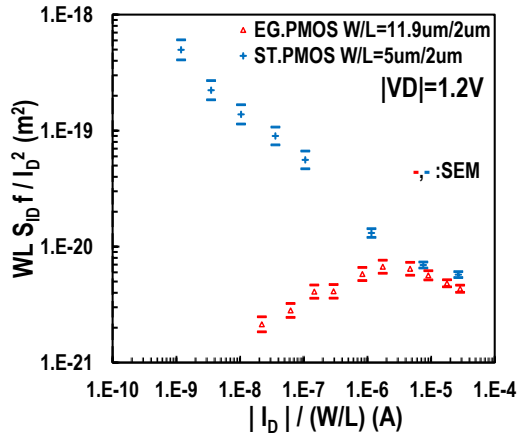
From the normalized standard deviation of the natural logarithm of  $1/f$  noise  $\ln(WLS_{IDf}/I_D^2)$  versus the inverse square root of the surface plots, we can observe the area dependence of noise variability which leads to a larger noise dispersion in smaller devices, in both PMOS and NMOS transistors, due to the presence of RTS noise. Also, the increased noise dispersion in lower levels of inversion is clear.

## 4.5 Comparison of LFN behavior in standard and enclosed gate MOSFETs

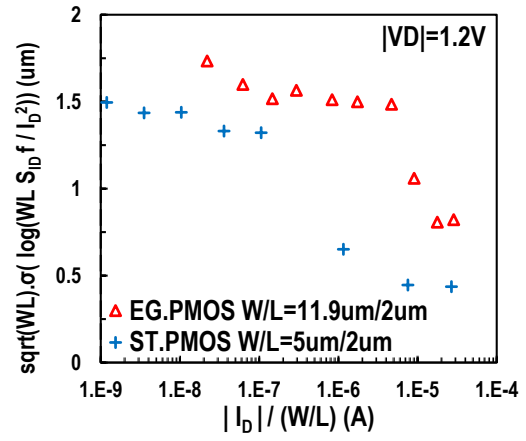
In this section a short comparison of LFN behavior between conventional MOSFETs and devices with enclosed gate layout will be presented. The LFN variability model that applied, is described by equation 3.15 and uses the normalized standard deviation of the logarithm of  $1/f$  noise  $\log(WLS_{IDf}/I_D^2)$ . In the figures above, the measured mean value of  $WLS_{IDf}/I_D^2$  versus  $|I_D|/(W/L)$  and the normalized standard deviation of the logarithm of  $1/f$  noise multiplied with the square root of the surface,  $\sqrt{WL} \cdot \sigma(\log(WLS_{IDf}/I_D^2))$ , for NMOS and PMOS devices with enclosed gate layout and conventional structure, with the same channel length ( $L=2\mu m$ ), are depicted.



**Figure 4.30** a) Measured mean value of  $WLS_{IDf}/I_D^2$  versus  $|I_D|/(W/L)$  and b) normalized standard deviation of  $1/f$  noise  $\log(WLS_{IDf}/I_D^2)$  multiplied with the square root of the surface  $\sqrt{WL}$ , for NMOS transistors with enclosed gate layout and conventional structure, with  $W/L=11.9\mu m/2\mu m$  and  $W/L=5\mu m/2\mu m$  respectively, at saturation region.

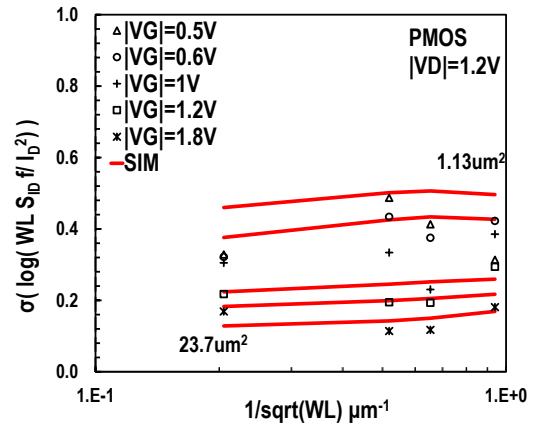
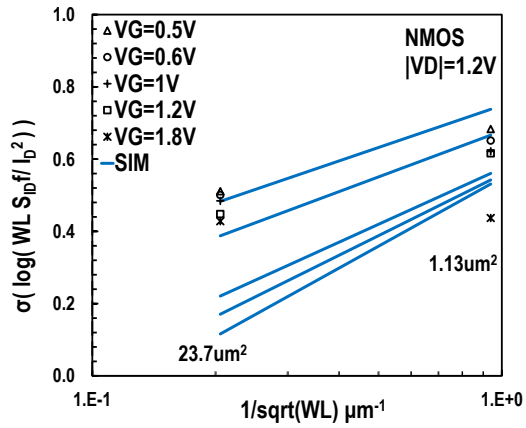


c)

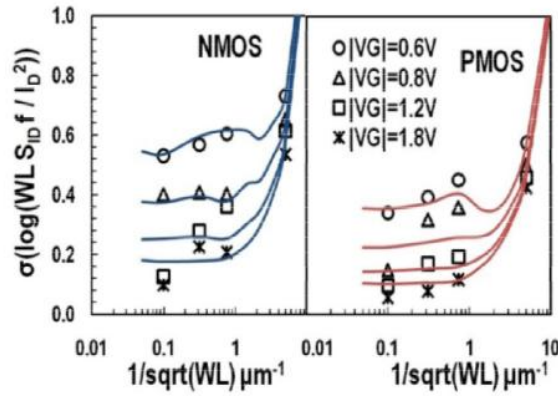


d)

**Figure 4.31** a) Measured mean value of  $WLS_{ID}f/I_D^2$  versus  $|I_D|/(W/L)$  and b) normalized standard deviation of  $1/f$  noise  $\log(WLS_{ID}f/I_D^2)$  multiplied with the square root of the surface  $\sqrt{WL}$ , for PMOS transistors with enclosed gate layout and conventional structure, with  $W/L=11.9\mu m/2\mu m$  and  $W/L=5\mu m/2\mu m$  respectively, at saturation region.



a)



b)



**Figure 4.32** Normalized standard deviation of the logarithm of  $1/f$  noise  $\log(WLS_{ID}/I_D^2)$  referred to 1 Hz versus the inverse square root of the surface for both NMOS and PMOS devices a) with enclosed gate layout and b) with conventional structure and  $L=2\mu m$  [15]. Measurements: markers, Model: lines.

Standard NMOS devices show a slightly decreased mean value of noise and reduced noise variability. On the other hand, in enclosed gate PMOS transistors, a significantly decreased noise level, compared with the standard PMOSFETs, can be observed especially in weak inversion. In this case noise variability presents slightly higher values than in standard devices. Furthermore, for typical MOSFETs we can clearly see the  $1/\sqrt{WL}$  dependence of LFN variability with the device area ( $WL$ ) (Figure 4.32 b)). In the case of the enclosed gate devices this trend can not be clearly observed. It should be mentioned though, that the smallest enclosed gate transistor area is above  $1\mu m^2$  whereas in the conventional MOSFET technology, devices with smaller areas ( $WL < 1\mu m^2$ ) are available.

Parameter	A	B
Units	$\mu m$	-
$_{EGNMOS}$	0.3	0.6
NMOS	0.11	0.98
$_{EGPMOS}$	0.06	0.15
PMOS	0.09	0.53

**Table 4.3**  $1/f$  noise parameters for a  $0.18\mu m$  conventional CMOS technology [15] and a  $0.18\mu m$  CMOS technology with enclosed gate layout. For the parameter extraction, the standard deviation of  $\log(WLS_{IDf}/I_D^2)$  was used.

In Table 4.3 the  $1/f$  noise parameters that extracted for a  $0.18\mu m$  CMOS technology for both standard [15] and enclosed gate transistors, using the  $\log(WLS_{IDf}/I_D^2)$  LFN variability model that described with equation 3.15, are presented. For both kind of devices statistical parameters A and B are relatively close exhibiting lower values in the case of enclosed gate MOSFETs.

# Chapter 5

## Conclusions

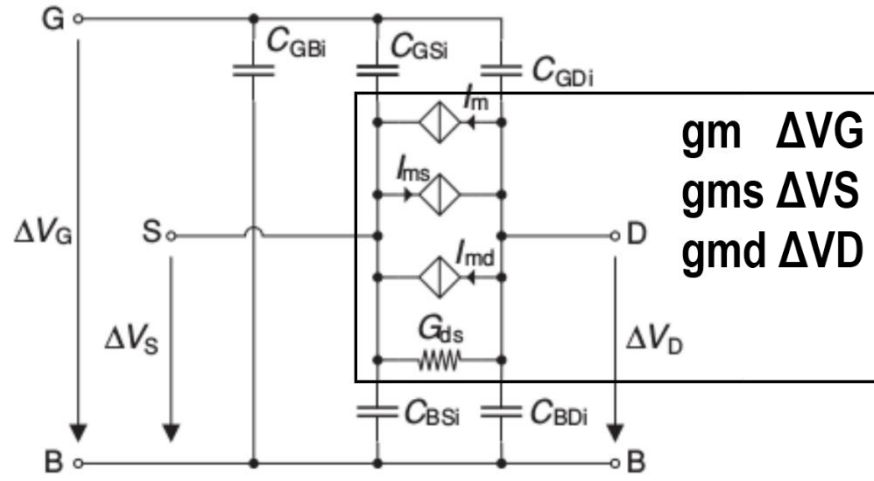
Within the context of this thesis, a detailed analysis of low frequency noise in enclosed gate MOSFETs, in a 0.18 $\mu$ m CMOS process, was presented for the first time. LFN was examined in PMOS and NMOS devices with geometries of, W/L=11.9 $\mu$ m/2 $\mu$ m, 7.42 $\mu$ m/0.5 $\mu$ m, 6.87 $\mu$ m/0.34, 6.29 $\mu$ m/0.18 $\mu$ m, and W/L=11.9 $\mu$ m/2 $\mu$ m, 6.29 $\mu$ m/0.18 $\mu$ m, respectively, in all regions of inversion for both linear and saturation region of operation. The results were evaluated under the carrier number fluctuation with correlated mobility fluctuations model and the basic bias and area related LFN variability model was used. Both models described adequately noise behavior for the studied enclosed gate MOSFETs. Enclosed gate NMOS devices show a higher variability than enclosed gate PMOS devices but lower noise levels. This is similarly as in standard transistors. Furthermore, enclosed gate PMOS devices, in weak inversion, show a reduce noise level at increased drain voltage. This noise reduction is interestingly accompanied by noise variability reduction.

The results of this thesis point to several interesting directions on future work. The I/V characterization and evaluation of LFN in enclosed gate MOSFETs, with a charged base model which takes into account the device special geometrical characteristics should be the next step. Furthermore, low frequency noise mismatch between paired devices within the same die and investigation of the deviation of LFN from the ideal 1/f slope, especially in weak inversion, are also two crucial subjects that should be examined.

# Appendix A

## A.1 MOS Transistor small signal equivalent circuit

In Figure A.1 the MOS small signal equivalent circuit is depicted [1]. The Source, Drain Gate and Bulk transconductances, are defined by equations A.1, A.2, A.3 and A.4 respectively.



**Figure A.1** MOS Transistor small signal equivalent circuit.

$$g_{ms} = +(-) \frac{\partial I_D}{\partial V_S} \quad (A.1)$$

$$g_{md} = +(-) \frac{\partial I_D}{\partial V_D} \quad (A.2)$$

$$g_m = +(-) \frac{\partial I_D}{\partial V_G} \quad (A.3)$$

$$g_{mb} = +(-) \frac{\partial I_D}{\partial V_{BS}} \quad (A.4)$$

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