



TECHNICAL UNIVERSITY OF CRETE
SCHOOL OF ELECTRONIC AND COMPUTER ENGINEERING
MICROELECTRONICS LABORATORY

“Study of Low Frequency Noise in High Voltage MOS Transistor”

Diploma Thesis
by

Constantinos Fellas

Committee:

Matthias Bucher, Assistant Professor (Advisor)
Costas Balas, Professor
Eytyxios Koutroulis, Assistant Professor

Chania, October 2014

Acknowledgements

Pursuing the diploma in Electronic and Computer Engineering field and after lots of endeavors while working with my diploma thesis in MOSFET Modelling, I realized that this work would never be fulfilled without the support of some people.

First, I am grateful to my advisor Professor Matthias Bucher, who gave me the opportunity to enter the unknown world of MOSFET modelling.

I would also like to express my sincere gratitude and appreciation to PHD candidate Nikolaos Mavredakis. Without his continuous guidance and encouragement, my research work towards this thesis would never be possible.

Finally I would like to thank my **FAMILY** for their support all this years and Aggelos Antonopoulos, Nikos Makris, Kostas Papathanasiou and Giorgos Gyroukis for the support in order to implement this thesis.

Abstract

HVMOSFETs find many different applications such as switching applications, input-output operations, voltage conversions, RF amplification etc. The effect of drift region on $1/f$ noise remained unclear until recently due to the difficulty of performing $1/f$ noise measurements under high drain voltages, on the order of tens of Volt. This is mainly due to the lack of adequate measurement equipment, which usually restricts low frequency noise to be measured up to just a few Volt, usually generated from batteries.

A $1/f$ noise parameter extraction method for high-voltage (HV-)MOSFETs at 3V drain bias is presented in this thesis. In this region the overall noise is mostly dominated by the noise originating in the channel. The bias dependence of flicker noise, related to transconductance-to-current ratio, allows for an easy means to determine related noise parameters. Though measured data is limited, parameters related to carrier number fluctuation effect may be found. 50 V N and P-channel HV-MOSFETs are investigated for long as well as short channel lengths. The parameter extraction method is applied to a recently established $1/f$ noise model for HV-MOSFETs, showing a good agreement among model and experimental data.

CONTENTS

Chapter 1 Introduction

1.1 Noise in general.....	5
1.2 Thesis structure.....	6

Chapter 2 High Voltage MOSFET Structure

2.1.1 General.....	7
2.1.2 Lateral-Diffused MOSFET (LDMOS).....	8
2.1.2 Vertical - Diffused MOSFET (VDMOS).....	9
2.2 DC behavior of HV - MOSFETs.....	9
2.2.1 High voltage effects.....	10
2.3 General description of the HV-MOSFET model.....	12

Chapter 3 Simple low frequency noise model and measurement analysis

3.1 Noise sources in MOSFET.....	14
3.2 Low Frequency noise simple model.....	15
3.2.1 Basic carrier number fluctuation effect.....	16
3.2.2 I - V Model.....	16
3.2.3 Basic carrier number fluctuation model.....	16
3.3 Measurements analysis.....	17
3.3.1 I-V and noise measurements results.....	18
3.3.2 I - V and noise simulation results.....	18

Chapter 4 Parameter extraction and model validation

4.1 Extraction of IV parameters.....	24
4.2 1/f noise parameter extraction.....	26
4.2.1 Extracted parameters for N-channel devices 350nm.....	27
4.2.2 Extracted parameters for P-channel devices 350nm.....	29
4.2.3 Bias Dependence analysis of 1/f noise - Model Validation.....	31

Chapter 5 Results and discussion.....

Appendix A.....

References.....

Chapter 1 Introduction

1.1 Noise in general

Noise means any unwanted sound. Noise is not necessarily random. Sounds, particularly loud ones, that disturb people or make it difficult to hear wanted sounds, are noise. For example, any unwanted sound such as domesticated dogs barking, kids playing, loud music, portable mechanical saws, road traffic sounds, or a distant aircraft in quiet countryside, is called noise.

In electronics, noise is a random fluctuation in an electrical signal, a characteristic of all electronic circuits. Noise generated by electronic devices varies greatly, as it can be produced by several different effects. Thermal noise is unavoidable at non-zero temperature, while other types depend mostly on device type such as shot noise, or manufacturing quality and semiconductor defects, such as conductance fluctuations, including $1/f$ noise.

In communication systems, noise is an error or undesired random disturbance of a useful information signal in a communication channel. The noise is a summation of unwanted or disturbing energy from natural and sometimes man-made sources. Noise is, however, typically distinguished from interference, (e.g. cross-talk, deliberate jamming or other unwanted electromagnetic interference from specific transmitters), for example in the signal-to-noise ratio (SNR) which is defined as the power ratio between a signal (meaningful information) and the background noise (unwanted signal) [1].

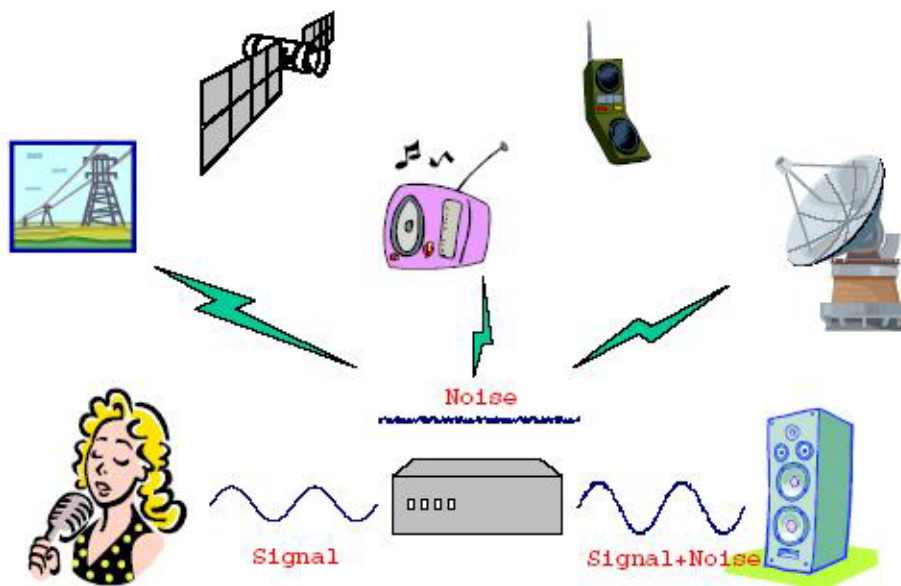


Figure 1.1 - Noise Sources

1.2 Thesis structure

This diploma thesis deals with Low Frequency noise in High Voltage MOSFETs. A short introduction about noise in electronics is presented in chapter 1.

In chapter 2 a short introduction to the operation as well as the structure of two of the most important HV - MOSFET devices, LDMOS and VDMOS will be presented. A brief analysis including DC characteristics and physical effects are also given in this chapter. We also describe in brief the HV MOSFET model which was built to describe the behavior of High Voltage MOSFETs.

In chapter 3, firstly noise sources in MOSFET are presented in a brief and then we focus on simple Low Frequency noise model and Measurements analysis.

We will discuss the main effect (Basic carrier number fluctuation) taking place in this simple model as well as I - V model characteristics. At the end of this chapter we provide plots from I - V and noise measurements analysis.

Chapter 4 dedicates on parameter extraction method. I - V and $1/f$ noise parameters equations are given and the parameter extraction method is presented analytically.

In Chapter 5 conclusions of this work are proposed and future work is suggested.

Chapter 2: High voltage MOSFET structure

2.1.1 General

A metal–oxide–semiconductor field-effect transistor (MOSFET) is based on the modulation of charge concentration by a MOS capacitance between a **body** electrode and a **gate** electrode located above the body and insulated from all other device regions by a gate dielectric layer which in the case of a MOSFET is an oxide, such as silicon dioxide. If dielectrics other than an oxide such as silicon dioxide (often referred to as oxide) are employed the device may be referred to as a metal–insulator–semiconductor FET (MISFET). Compared to the MOS capacitor, the MOSFET includes two additional terminals (**source** and **drain**), each connected to individual highly doped regions that are separated by the body region. These regions can be either p or n type, but they must both be of the same type, and of opposite type to the body region. The source and drain (unlike the body) are highly doped as signified by a "+" sign after the type of doping. HV-MOSFET are widely used as power devices, especially in monolithic systems which are comprised of both power and logic circuitry, because the technology is compatible with the standard CMOS process. Moreover, HV-MOSFETs exhibit a fast switching ability and negative temperature coefficient of the drain current which eases various problems like thermal runaway, secondary breakdown and current crowding. Many different HV-MOSFET devices structures have been proposed including but not limited to double-diffused MOSFETs (DMOS), V-groove MOSFETs (VMOS) and trench - gate MOSFETs (UMOS). DMOS devices, which are the most important HV-MOSFET structures can be further separated into lateral-diffused (LD) and vertical-diffused (VD). [3]

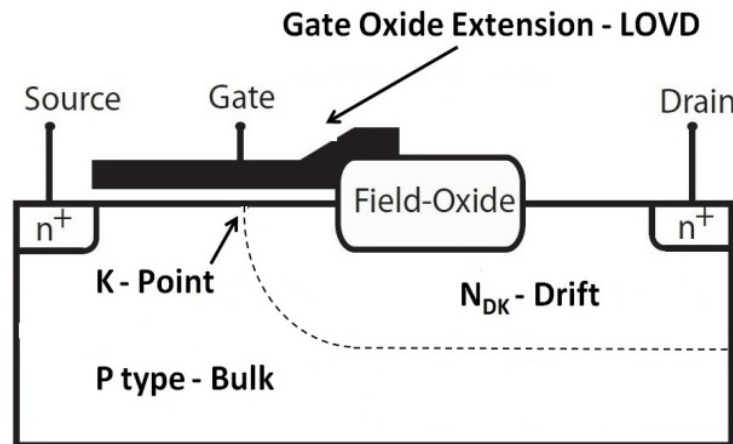


Figure 2.1 - Schematic of an HV-MOSFET

2.1.2 Lateral-Diffused MOSFET (LDMOS)

As CMOS technology is maturing in deep-submicron lithography, other approaches were investigated in order to make available high voltage devices with improved characteristics. The LDMOS device architecture, which actually originated from DEMOS/LDD-MOS, has much higher breakdown voltage than DEMOS architectures. Figure 2.2 shows the schematic representation of N-type LDMOS device. The LDMOS devices are useful in high-voltage switching because of their switching speeds and relative simplicity in processing. There are many variations of LDMOS devices. The device shown in Fig 2.2 is generally used for 20-100V application e.g. switch-mode power supplies and power amplifiers etc. The channel in the device is created using double diffused process and thus it has lateral non-uniform doping. The effective gate length is shorter than the physical length of the gate electrode. The drift region is lightly doped N-type whose length varies with increasing voltage blocking capability in the drain side. The maximum drain-source voltage, that can be applied, is determined by the breakdown voltage of the p-n junction, which is limited by the n layer doping, thickness and field crowding at the junction edge.

The electric field in the LDMOS near the silicon surface is considerably lower than in the conventional MOS. However, the maximum field still remains on the surface and avalanche breakdown may occur there. The surface electric field can be reduced significantly by the use of thick oxide (as shown in Fig. 4) or field plate as the maximum field is now located inside the bulk. To reduce the on-resistance in LDMOS (with field plate), the length of the field plate should be as small as possible. The effect of field plate on LDMOS characteristics e.g. breakdown-voltage, quasi-saturation effect has been studied in the literature in detail. The on-resistance of the LDMOS can also be decreased by using ion-implantation in the drift region. The field plate also shields the gate from the drain potential, thus minimizing the feedback (drain-to-gate) capacitance, which means improvement of RF signal gain. The p-n junction and the field plate form a fairly uniform field between gate and the drain, thus giving better breakdown voltage.

The LDMOS transistors fare much better at higher frequencies compared to their vertical counterpart (VDMOS) devices. The LDMOS transistors with frequencies more than 2.7GHz are already available in the market. Since in the LDMOS design, the gate, source and drain are all on the top surface, chip size grows rapidly for high voltage handling capability above 200V.[3]

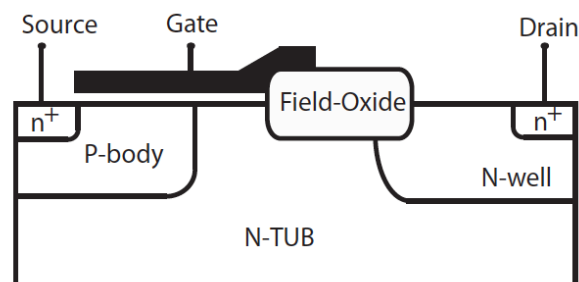


Figure 2.2 - Schematic representation of the Lateral double - Diffused MOSFET (LDMOS)

2.1.2 Vertical - Diffused MOSFET (VDMOS)

The growing chip size problem for higher operating voltages is addressed by the VDMOS transistor technology. Fig. 2.3 shows the schematic representation of N-type VDMOS device. Since these devices have the drain at the back surface, a variety of junction edge termination schemes can be utilized at the perimeter of the die. However, the channel region itself is on the top surface and thus the current flow is lateral through the channel and vertical through the lightly doped drift. The channel in the device is created using double diffused process and thus it has lateral non-uniform doping. The effect of lateral non-uniform doping and lightly doped drift region on device characteristics is explained in the next section. The VDMOS design sacrifices speed for lower on-resistance and denser high-voltage layout due to large gate/drift overlap[3].

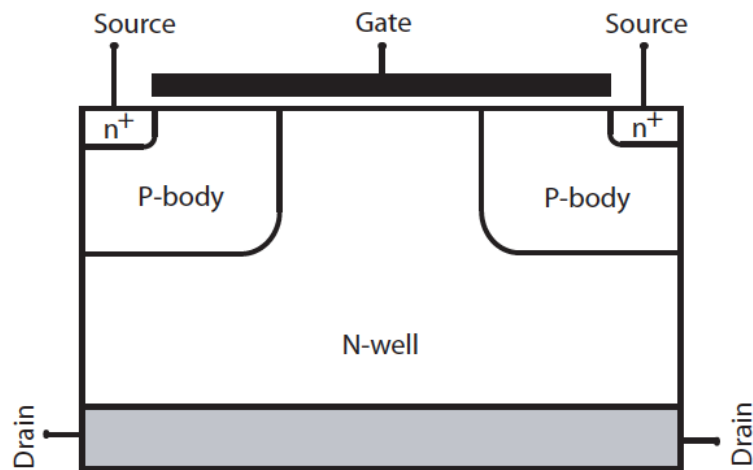


Figure 2.3 - Schematic representation of the Vertical double - Diffused MOSFET (VDMOS)

2.2 DC behavior of HV-MOSFETs

The high voltage devices show some special effects due to high electric field inside the device e.g. self-heating, quasi-saturation and impact ionization effects. In fact, some of these effects (self-heating and impact ionization) are also visible in low voltage MOSFETs as electric field in these devices also becomes quite high as channel length is decreased[3]. The K point (intrinsic drain)[5], voltage provides a powerful and robust criterion for the separation between the different saturation mechanisms (figure 2.4). It should be mentioned, several effects may be superposed in the same time on the electrical characteristics of a HV device.

Some Effects that

We will differentiate two saturation mechanisms:

- saturation
- quasi-saturation and

four other effects:

-impact ionisation, drift pinch-off, dipole charge built-up and self-heating
Even though above mentioned effects arise due to high electric fields in the device, some other special effects are also observed due to different device processes in these devices compared to conventional MOSFETs. One of the major difference in terms of device process is the lateral non-uniform doping in the channel and drift region in the drain side of HV devices. Here we will discuss the physical origin of these effects and their impact on device characteristics.

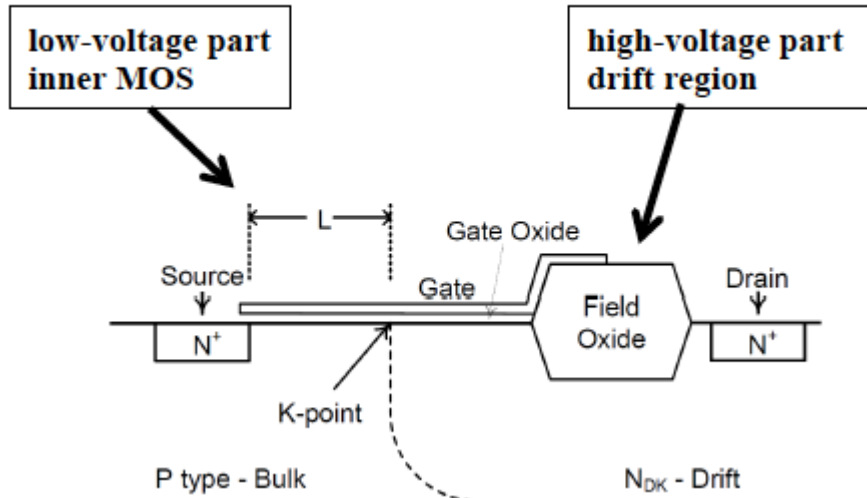


Figure 2.4 - Typical Structure HV-MOS

2.2.1 High voltage effects

The quasi-saturation effect is one of the unique effect observed in HV devices other than bipolar devices. To explain the quasi-saturation effect, first let's discuss the saturation mechanisms in HV devices using output characteristics of LDMOS transistor shown in Figure 4. The current saturation on $I - V$ characteristics can occur due to following three mechanisms:

(a) Pinch-off in the channel

For a fixed gate voltage, if drain voltage is increased, the channel gets depleted and current saturates. This effect is called pinch-off and it is also the normal saturation mechanism in long channel MOSFETs. In HV devices, the channel pinch-off is generally observed at low V_{GS} . [3,4]

(b) Velocity saturation in the channel:

If the lateral electric field in the channel is more than certain limit called as critical field, the velocity of the electrons get saturated and thus there will be no further increase in the current for any further increase in the drain voltage. This effect is called velocity saturation, which is quite common phenomenon in short channel MOSFETs. In HV devices, this effect is generally observed for medium to high V_{GS} . A simple way to see this effect is that when

intrinsic MOS is velocity saturated, the output characteristics become equidistant for equal increase in V_{GS} .[3,4]

(c) Velocity saturation in the drift region

Another saturation mechanism can occur due to velocity saturation in the drift while intrinsic MOS is still not saturated. Actually this cannot be called saturation as current does not get saturated. If drift is velocity saturated and intrinsic MOS is in linear region, the increase in V_{GS} does not increase current level significantly and gate bias has no or little effect. This effect is called quasi-saturation, which is generally observed at high V_{GS} . Note that all or any two of the three effects described above may superimpose with each other and, sometimes, they may not be separable from each other.[3,4]

(d) **The self-heating effect (SHE)** represents the heating of the device due to its internal power dissipation. This effect appears, when high levels of power are attained in the device. The dissipated heat leads to an increase in the internal temperature of the device and modifies the $I - V$ characteristics. The decrease in the current with increasing V_{DS} is caused by the self heating effect. As V_{DS} increases, the current starts rising. The increase in the current (I_{DS}) as well as voltage across the device (V_{DS}) increase the power dissipation ($I_{DS} V_{DS}$) inside the device. As discussed above, the increase in power dissipation increases temperature which affects other transistor parameters. The rise in temperature decreases mobility due to scattering which in turn decreases the current showing negative resistance on output characteristics.

The internal temperature increase due to self heating effect influences the device characteristics mainly by affecting the mobility, threshold voltage and velocity saturation. In the literature, this effect was mainly studied on the SOI devices and the proposed models for SHE are distributed or non-distributed models. [3 , 4]

(e) Impact Ionization Effect

In Low Voltage, the increase in the V_{DS} in the MOSFET increases the longitudinal electric field in the channel increasing from source to drain. For abrupt source and drain junctions, the peak field is at the drain-to-channel junction, and its value depends on V_{DS} and channel length L . When carriers move in the fields that exceed the value of the onset of velocity saturation, they continue to acquire kinetic energy from the field but their velocity is randomized by the excessive collisions such that their velocity along the field direction no longer increases but their kinetic energy does. Depending on the statistics of scattering, a small fraction of the overall carrier population acquires a significant amount of energy, and these are called hot carriers. Clearly, the higher the field, the higher the proportion of hot carriers. Generally, in MOSFETs, the high fields are encountered in saturation in the pinch-off region. The new electrons join the stream of channel electrons and move toward the drain.

The impact ionization in the HVMOS device has the contributions from both the channel region and the drift region. At low current, the hot carriers are generated near the channel while at high current levels, hot carriers are generated near the drain end in the drift region.

This is why there is an increase in the I_{DB} at higher V_{GS} . [3,4]

2.3 General description of the HV-MOSFET model

The EPFL HV-MOSFET model is a compact model built to describe the behaviour of High Voltage MOSFETs. It is made to cover both Lateral double-Diffused (LD) MOS and Vertical double-Diffused (VD) MOS devices. The development of the model is the result of a lengthy, and also ongoing, research on the HV-MOS devices performed at EPFL with collaboration with other organizations.

The HV-MOS devices can be analyzed as the in-series combination of two simpler compounds, one for the low-voltage part and one for the high-voltage part[3]. This is illustrated at the simplified sketches presented at Figure 2.5

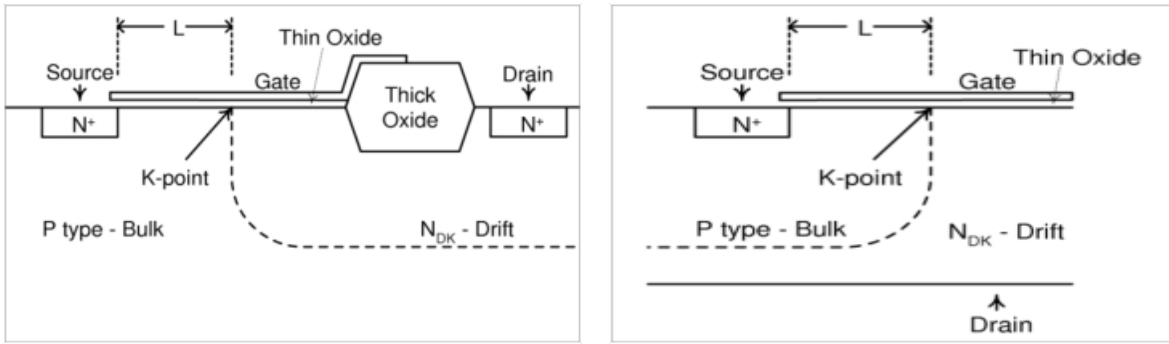


Figure 2.5 - Simplified sketches of an LDMOS (a) and a VDMOS (b) device. The HV-MOS device can be analyzed into two parts: one low-voltage part, between the Source and the K-point and one high-voltage part, between the K-point and the Drain.

Following this approach a macromodel can be built that will describe the HV-MOS device as a whole. The two parts of the macromodel will be described by two separate compact models. This macromodel approach is illustrated in Figure 2.6

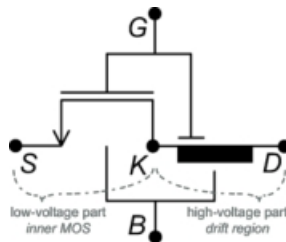


Figure 2.6 - The macromodel describing the HV-MOSFET. The low-voltage part of the device is referred to as the inner MOS while the high-voltage part is labelled drift region. A separate compact model will be used for the description of each component.

The low-voltage part of the model is an inner MOS of the device. This part can be addressed using any compact model for MOSFETs. However, there are special characteristics in this case that should be taken into account.

For the high-voltage part of the device a novel physics-based approach has been developed.[5] According to this, the drift region is considered as a single dimensional problem and, with the help of a series of approximations, the system consisting of the Poisson's equation, the drift-diffusion current model and the Boltzmann's equation is managed to be solved analytically with respect to the current.

Chapter 3: Simple low frequency noise model and measurement analysis

3.1 Noise sources in MOSFET

The most important sources of noise in HV MOSFET are Thermal noise, flicker noise, shot noise and NQS noise.

- **Thermal noise** arises from the thermodynamic fluctuations of electron density in a material at any finite temperature. It is not expected thermal noise to be constant up to indefinitely high frequencies, as this would imply an infinite noise power, which is physically impossible. As every electronic device has non-zero resistance, thermal noise is therefore unavoidable, but it can be minimized through good device design[2].

- **Shot noise** comes from the fluctuations arising from carriers independently and randomly surmounting or crossing a barrier. The name comes from the notion that when listened to on a speaker, the noise source sounds similar to the volley of shots coming from a fired shot gun. It is typically dominant in devices like diodes and bipolar junction transistors, where current is produced by driving carriers over a barrier[2].

- **Flicker noise** as its name suggests, is characterized by a PSD that is inversely proportional to frequency. It therefore mainly dominates at low frequency, below the so-called corner frequency f_c , Fig 1.2, defined as the frequency at which $1/f$ noise contributes equally than the channel thermal noise to the total noise PSD (referred indifferently at the drain or at the gate). Because the $1/f$ noise scales inversely proportional to the gate area, it is becoming a major issue for analog IC design in deep and ultra-deep submicron devices. [12]

-**Non-Quasi Static or NQS noise** it is thermal noise which is mainly dominates above quasi static high frequency.

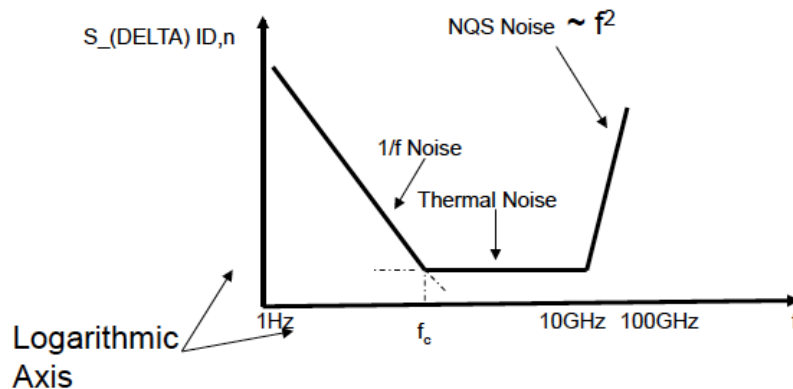


Figure 3.1 - The most important sources of noise in HV MOSFET

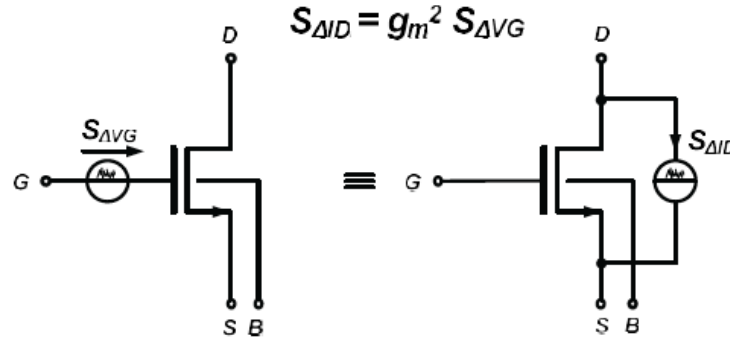
3.2 Low frequency noise simple model

Modeling of low frequency noise (LFN) in High-Voltage MOSFETs remains a critical issue in advanced HV CMOS technologies. A new complete charge-based HV-MOSFET model covering DC, RF and 1/f noise behavior has been recently established [5]-[8].

According to the flicker noise model [8] and other recent work [9]-[11], some noise mechanisms are attributed to the extension of gate oxide in the drift region, especially under low drain voltage conditions. The main contribution still comes from the channel region. We interpret the results using a standard approach, assuming that the noise generated in the device originates from carrier number fluctuations.

Flicker noise models, in their simplest form, assume a constant gate referred power spectral density (PSD) of gate voltage noise, and the equivalent power spectral density of noise at the drain is expressed as,

$$S_{\Delta I_D^2} = g_m^2 S_{\Delta V_G^2} \quad (1)$$



2

Fig. 3.2 Flicker noise of represented either as a noise voltage source at the gate or, equivalently, as a noise current source at the drain

3.2.1 Basic carrier number fluctuation effect

Carrier number fluctuations in the channel are thus induced by the electron capture/release, occurring near-at the Si/SiO₂ interface. The carrier number fluctuation effect is the dominant flicker noise source especially in moderate and early strong inversion region for low voltage (LV) MOSFETs [12]-[15]. The carrier number fluctuation effect is basically caused by the trapping/de-trapping effect in the oxide as well as by the Coulomb scattering mechanism which influences the mobility of the device. When the noise originates from number fluctuations, which is often the case, an increase in C_{ox} of the devices is predicted to reduce the LFN level [14]. This follows from the widely used approach to the LFN in the MOSFETs, involving McWhorter's model of charge exchange between the channel and oxide (border) states by tunnelling, with a characteristic length constant A [13].

3.2.2 I - V model

It is essential to have a correct dc model in order to implement a 1/f noise model, since certain quantities of the dc model, such as transconductance (G_M), slope factor (n), specific current (I_{SPEC}) and electron mobility (μ), are used in the noise equations. Transconductance-to-current ratio ($G_M U_T / I_D$) shown in is very helpful in the extraction of these dc parameters. This procedure is presented in detail in the chapter 4.

3.2.3 Basic carrier number fluctuation model

The basic carrier number fluctuation model in the channel region is described by the following equation [10],[11]:

$$\left. \frac{S_{I_D}}{I_D^2} \right|_{\Delta V} = \frac{kTq^2 N_T \lambda}{WLC_{ox} f} \left(\frac{G_M}{I_D} \right)^2 \left[1 + \alpha_C \mu C_{ox} \frac{I_D}{G_M} \right]^2 \quad (2)$$

Two basic parameters describe this effect: N_T which shows the number of trapped charges per unit area, and α_C which is the Coulomb scattering coefficient [12], [13]. Recent work has provided a general methodology for extracting these two parameters in LV CMOS devices [14] where λ is the tunneling attenuation distance equal to 0.1 nm.

The spectral dependence of LFN is considered here to be reasonably close to 1/f. Of course things are somewhat more complicated, but this formula can be considered sufficient for a first evaluation of LFN parameters.

3.3 Measurements analysis

In the present work, flicker noise was measured on 50 V N and P channel HV-MOSFETs with $T_{ox} = 15$ nm of the 0.35 μm HVC MOS technology from ams AG. The frequency range is from 10 Hz up to 100 kHz. The width of each transistor is $W = 40 \mu m$ while the channel length is $L = 10 \mu m$ for long devices, and $L = 500$ nm for short devices. The measurements are performed at 8 different drain current points for both transistors ($I_D = 1, 2, 5, 10, 20, 50, 100, 200 \mu A$) at a constant drain bias of $V_D = 3$ V. (as it shows table 1 below) Five different packaged samples were measured for each device, and an average of noise was calculated (Table 2) MATLAB, implementation code can be found in Appendix. The measurement setup in the present work limits drain bias; we assume that channel contribution in 1/f noise will be dominant. The current range covers a wide operation area from moderate inversion to (lower end of) strong inversion, where carrier number fluctuation is the main noise contributor.

For data analysis we used IC-CAP, a device modeling simulator from Agilent Technologies and Cadence spectre circuit simulator. Below we present a table (3.2.1) with drain currents used for measurements as well as another (table 3.2.2) with extracted gate voltage noise.

id (A) for NMOS50M and NFETI50T	id (A) for PMOS50M and PFET50T
2.00E-004	-2.00E-004
1.00E-004	-1.00E-004
5.00E-005	-5.00E-005
2.00E-005	-2.00E-005
1.00E-005	-1.00E-005
5.00E-006	-5.00E-006
2.00E-006	-2.00E-006
1.00E-006	-1.00E-006

Table 3.2.1 - Drain currents used for measurements

NMOS50M (H35) W=40um, L=10um (V)	PMOS50M (H35) W=40um, L=10um (V)	NMOS50M(H35) W=40um, L=500nm (V)	PMOS50M (H35) W=40um, L=1um (V)	NFETI50T (H18) W=40um, L=10um (V)	PFET50T (H18) W=40um, L=10um (V)	NFETI50T (H18) W=40um, L=200Nm (V)	PFET50T (H18) W=40um, L=200Nm (V)
2.0646	-2.981	1.1592	-1.5582	1.0596	-2.038	0.61732	-0.6378
1.6794	-2.3484	1.0658	-1.3776	0.8507	-1.505	0.56646	-0.5626
1.3998	-1.913	0.99488	-1.2466	0.6987	-1.15	0.52408	-0.5045
1.1708	-1.567	0.9287	-1.1328	0.57248	-0.8705	0.4811	-0.4490
1.0402	-1.3792	0.88328	-1.0674	0.4979	-0.7194	0.4503	-0.4110
0.9481	-1.2456	0.8439	-1.0154	0.44226	-0.6115	0.4213	-0.3770
0.85746	-1.1178	0.7955	-0.95718	0.3837	-0.5075	0.38444	-0.3355
0.81288	-1.0596	0.7658	-0.9280	0.3531	-0.4605	0.3613	-0.3105

Table 3.2.2 - Average of gate voltage noise for all MOSFETs

3.3.1 I-V and noise measurements results

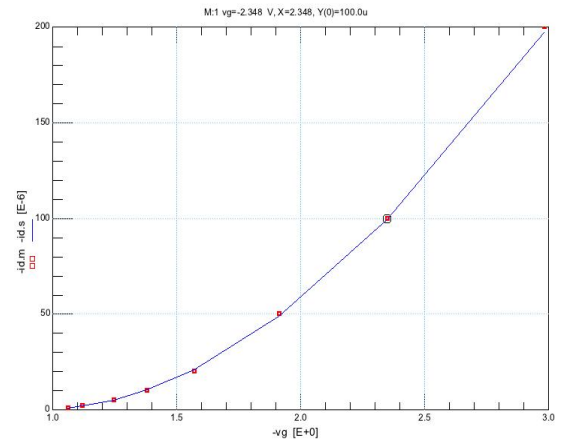
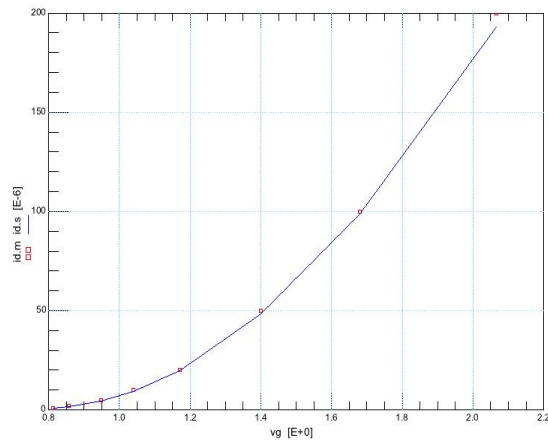
For each set, wide/long and wide/short N and P HV - MOSFETs that we measured we provide 6 plots for: id versus vg, log(id) versus vg, Noise versus Frequency, V_{noise} versus Frequency.

In below plots red color represents measurements and blue color the simulated model.

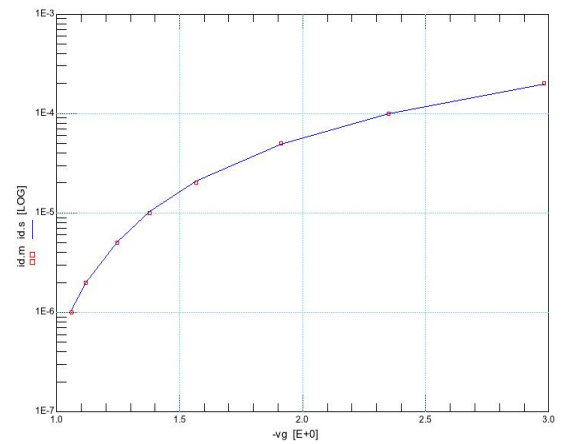
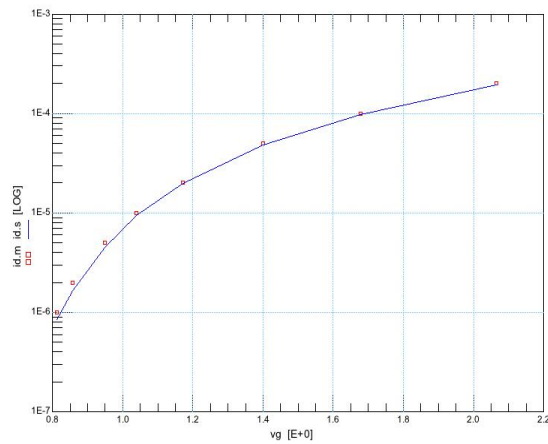
3.3.2 I - V and noise simulation results

-NMOS and PMOS 350nm W=40um L=10um I - V simulations

Id versus Vg

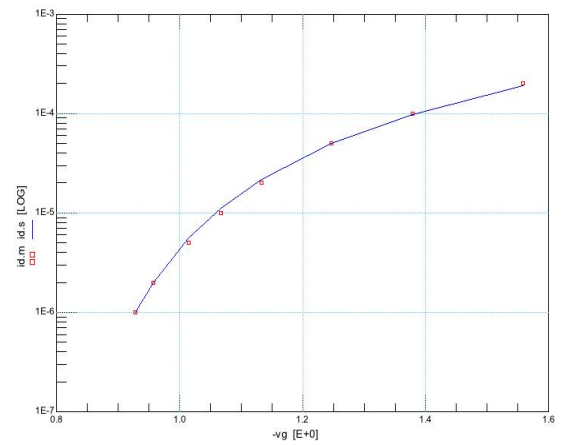
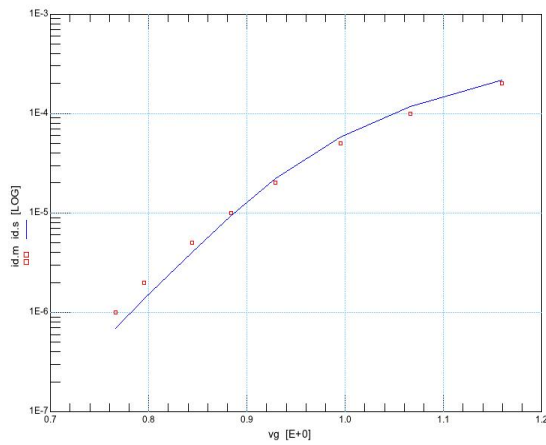
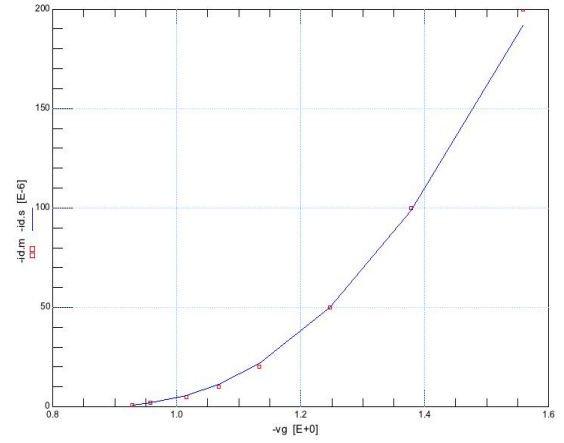
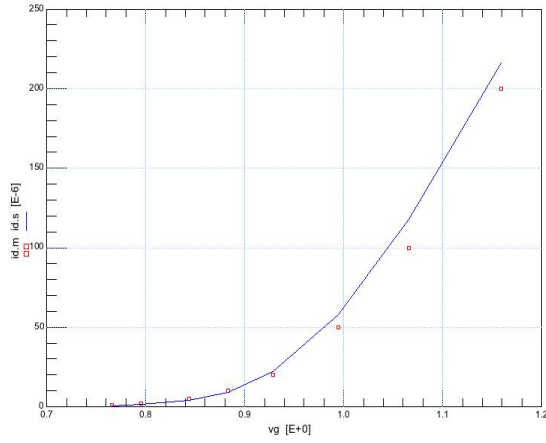


log(I_d) versus Vg



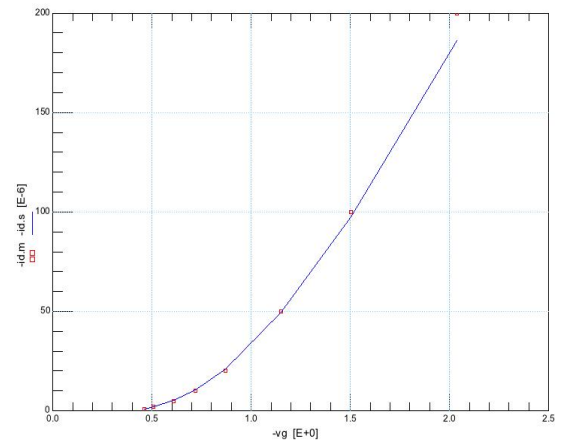
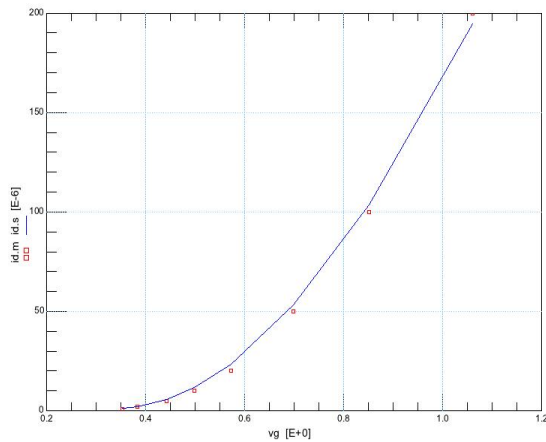
- NMOS and PMOS 350nm W=40um L=500nm/1um I - V simulations

Id versus Vg

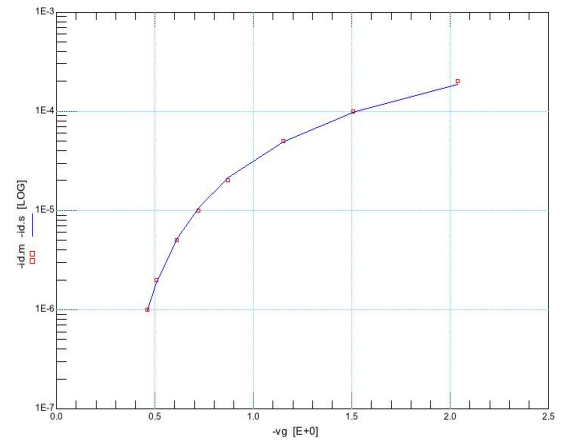
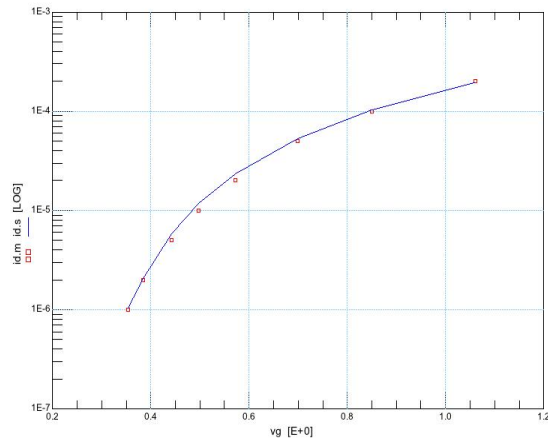


- NMOS and PMOS 180nm W=40um L=10um I - V simulations

Id versus Vg

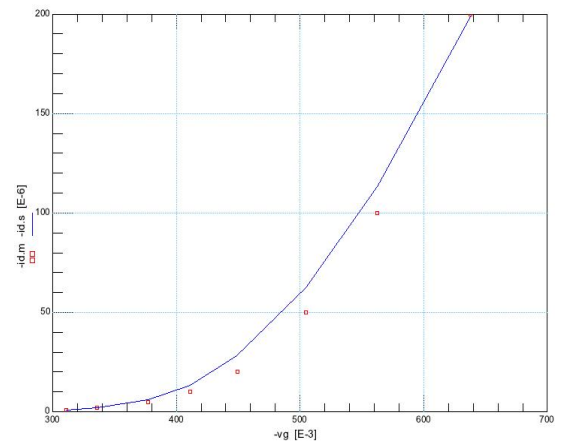
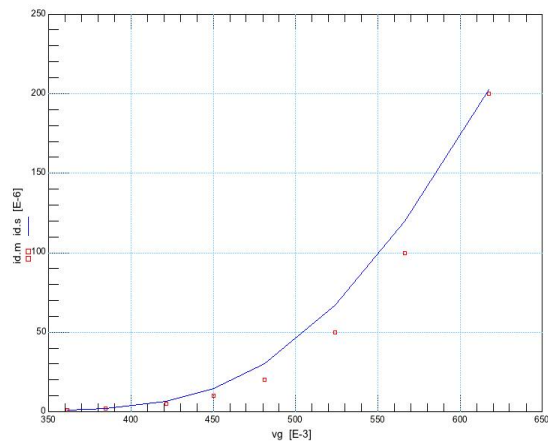


log(Id) versus Vg

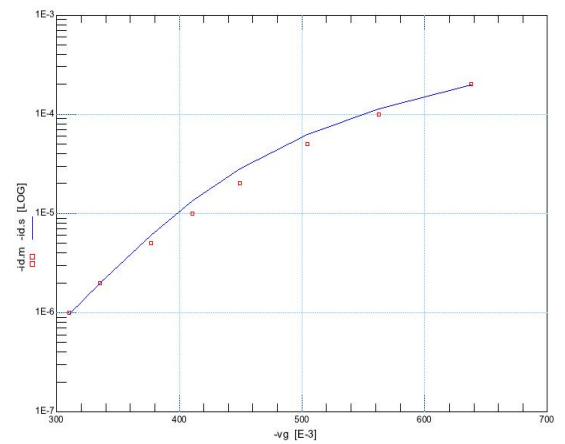
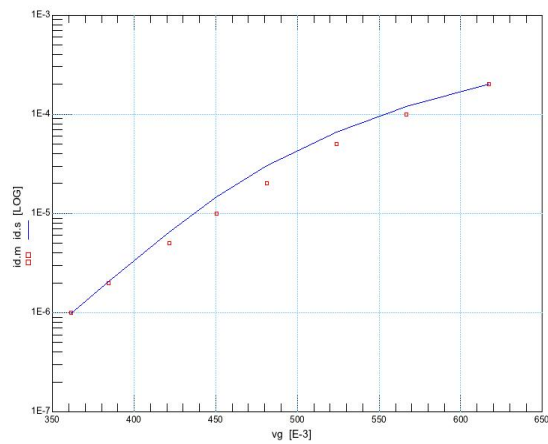


- NMOS and PMOS 180nm W=40um L=200nm I - V simulations

I_d versus V_g

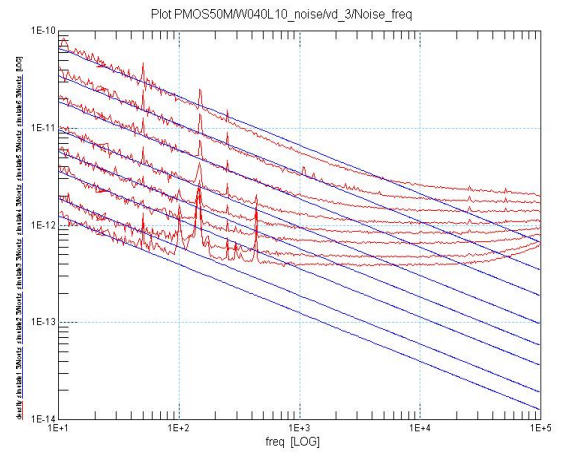
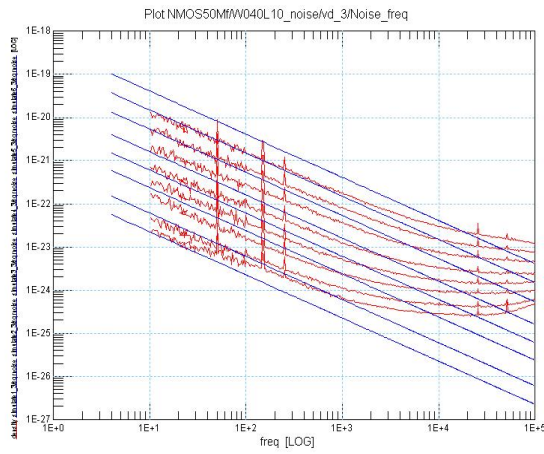


log(Id) versus Vg

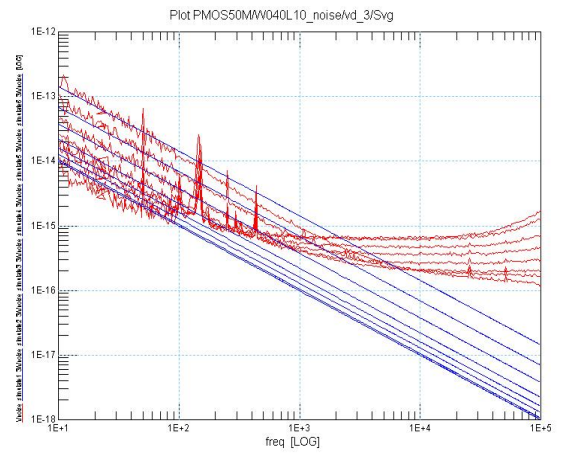
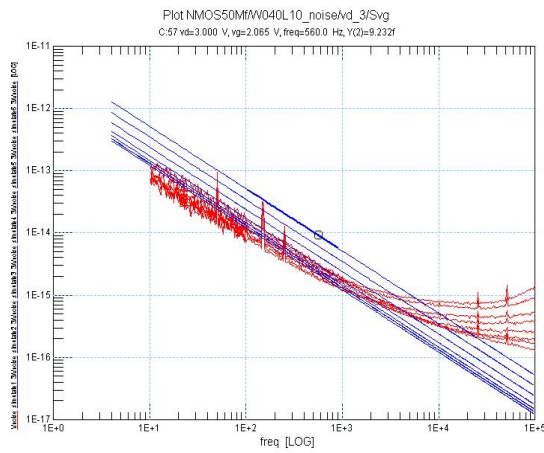


-NMOS and PMOS 350nm W=40um L = 10um 1/f simulations

Noise vs Frequency

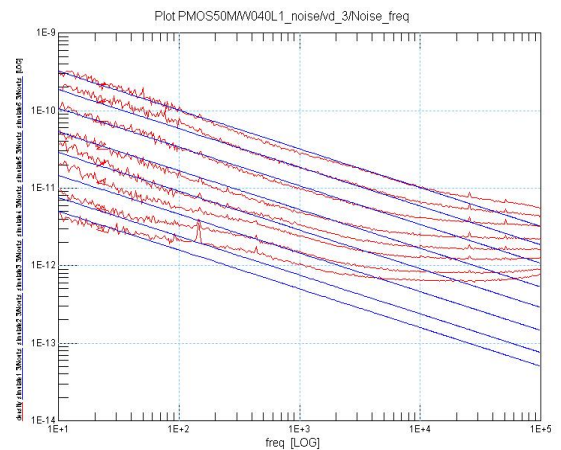
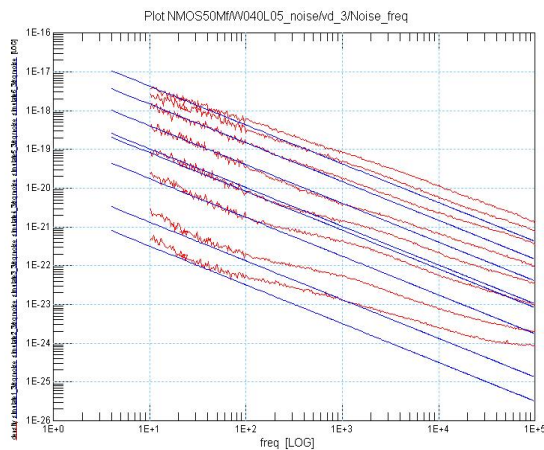


Svg vs Frequency

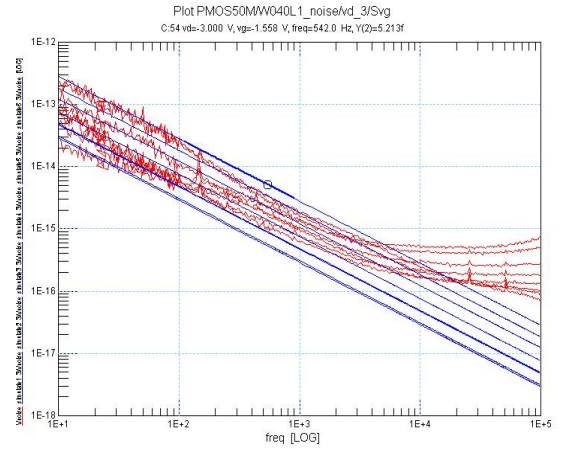
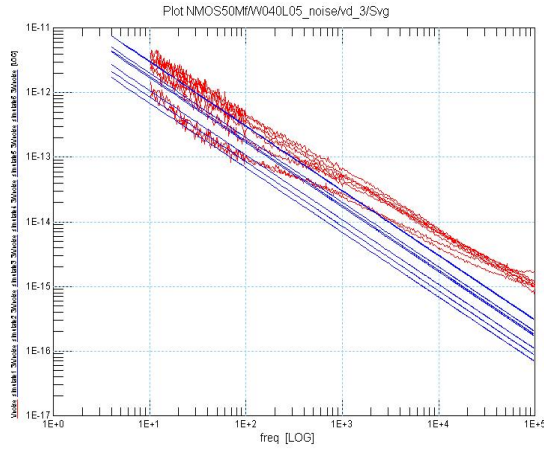


-NMOS and PMOS 350nm W=40um and L=500nm/1um 1/f simulations

Noise versus Frequency

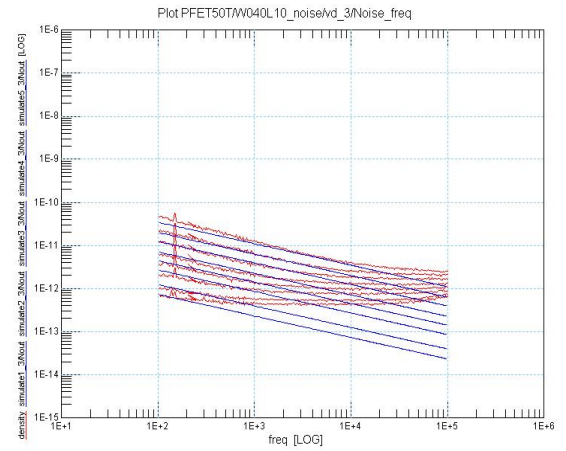
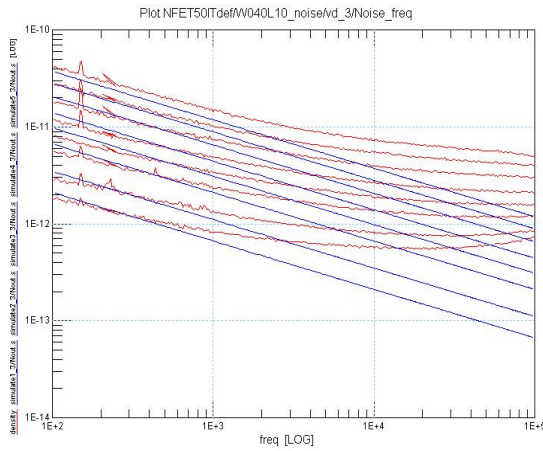


Svg vs Frequency

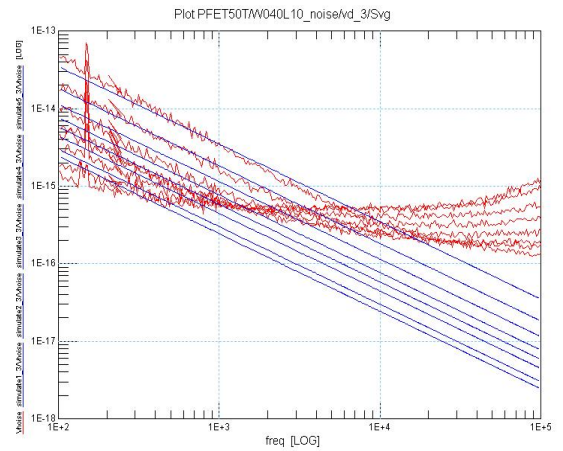
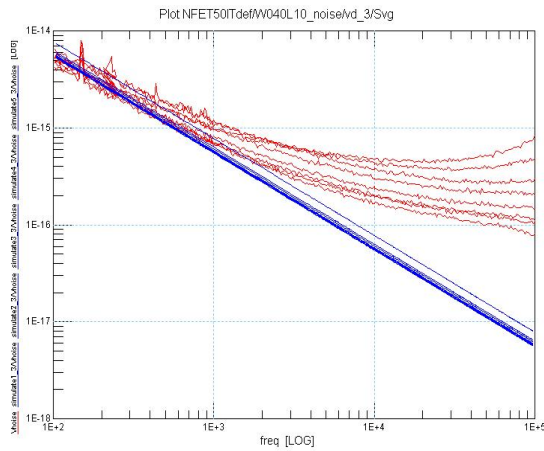


- NMOS and PMOS 180nm W=40um L=10um 1/f simulations

Noise versus Frequency

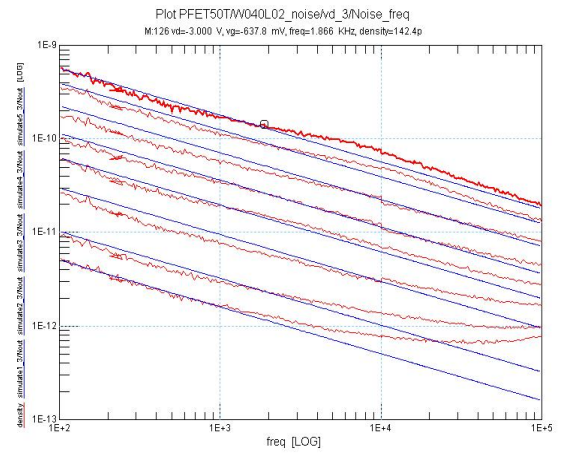
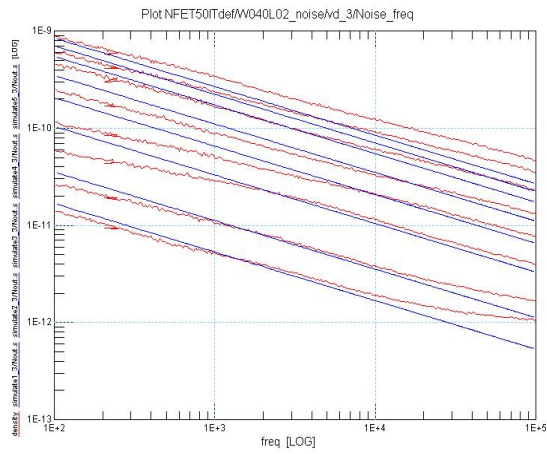


Svg vs Frequency

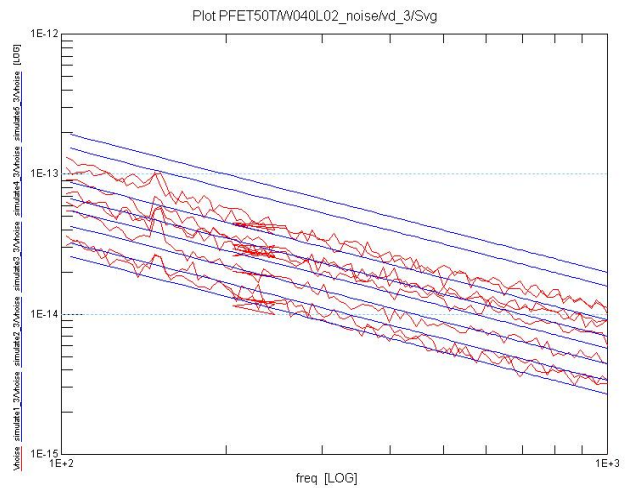
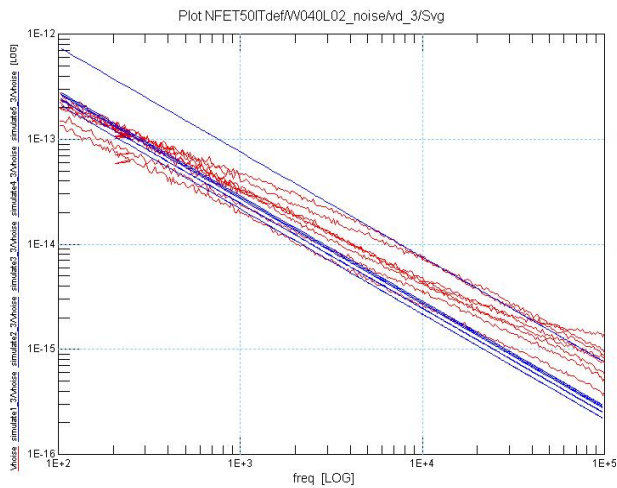


- NMOS and PMOS 180nm W=40um L=200nm 1/f simulations

Noise versus Frequency



Svg vs Frequency



Chapter 4: Parameter extraction and model validation

Starting from CV-IV data, fundamental quantities, such as I_{spec} are calculated [17], which are then used in noise equations for parameter extraction. In Fig. 4.1 the power spectral density S_{ID} is shown both for the measurements and the model [8]. The consistency of the model is good for all bias conditions.

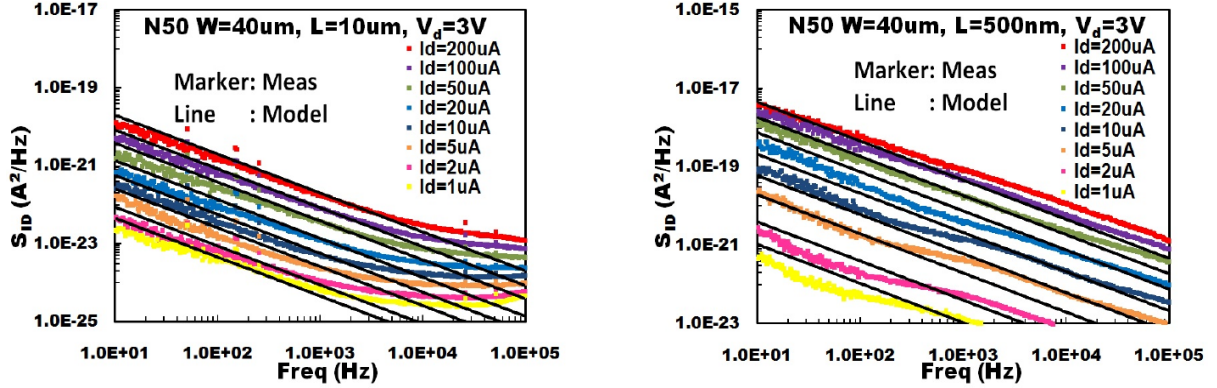


Fig. 4.1 - Power spectral density of drain current noise S_{ID} for 50 V long and short N-channel HV-MOSFETs, at $V_D = 3$ V for 8 different I_D values from 1 μ A to 200 μ A.

4.1 Extraction of IV parameters

As we mentioned above, it is essential to have a correct dc model in order to implement a $1/f$ noise model, since certain quantities of the dc model, such as transconductance (G_M), slope factor (n), specific current (I_{SPEC}) and electron mobility (μ), are used in the noise equations. In order to calculate the noise these quantities must be extracted first. G_M can be calculated as the derivative of the measured drain current. For obtaining n , I_{SPEC} , and μ , a specific procedure must be followed [18]. Transconductance-to-current ratio ($G_M U_T / I_D$) shown in Fig. 4.2 is very helpful in the extraction of these dc parameters. In the weak inversion regime n can be calculated as:

$$n = \frac{1}{(G_M U_T) / I_D} \bigg|_{\max} \quad (1)$$

while again from the transconductance to current ratio plot, I_{spec} corresponds to the current where $G_M U_T / I_D$ equals 0.616 of its maximum value [16]. Specific current is defined as,

$$I_{SPEC} = 2n U_T \mu C_{ox} \frac{W}{L}, \quad (2)$$

and given that oxide thickness is known as mentioned above, electron mobility can be easily calculated. Fig. 4 shows a general flowchart of the parameter extraction procedure where the first three blocks refer to IV parameter extraction.

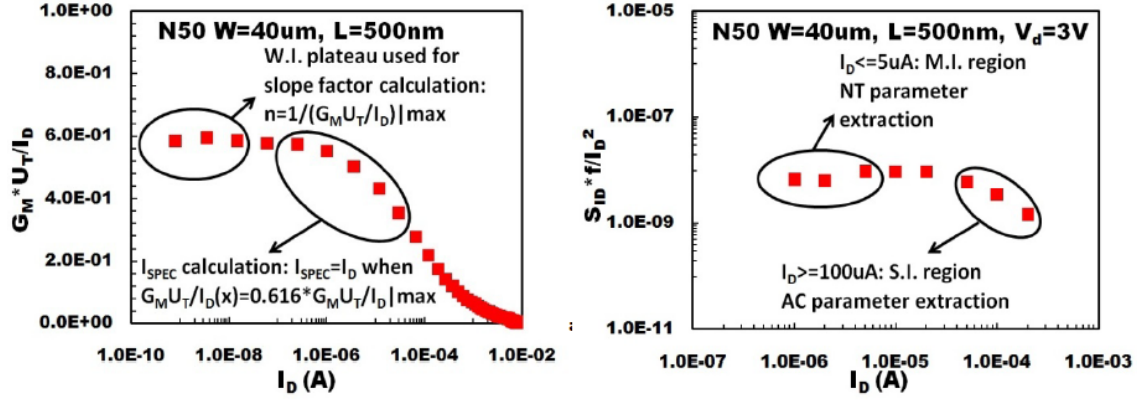


Fig. 4.2 - 1) Transconductance-to-current ratio versus I_D , 2) $1/f$ noise power spectral density referred to 1 Hz and divided by I_D^2 , versus I_D , for a short-channel NMOS 50V device.

4.2 1/f Noise parameter extraction

The basic carrier number fluctuation model in the channel region is described by the following equation [9],[10]:

$$\left. \frac{S_{I_D}}{I_D^2} \right|_{\Delta V} = \frac{kTq^2 N_T \lambda}{WLC_{ox}^2 f} \left(\frac{G_M}{I_D} \right)^2 \left[1 + \alpha_C \mu C_{ox} \frac{I_D}{G_M} \right]^2 \quad (3)$$

where λ is the tunneling attenuation distance equal to 0.1 nm.

The spectral dependence of LFN is considered here to be reasonably close to $1/f$. Of course things are somewhat more complicated [8], but this formula can be considered sufficient for a first evaluation of LFN parameters. Fig. 4.2.2 shows the bias dependence of $1/f$ noise referred to 1 Hz. In all cases the normalization was applied from 10 Hz to 1 kHz. Each noise parameter, N_T , and α_C , can be extracted from different inversion levels. For $I_D < 5\mu A$ in the moderate inversion region the second term of equation (3) can be neglected so that:

$$\left. \frac{S_{I_D}}{I_D^2} \right|_{\Delta V} \equiv \frac{kTN_T \lambda}{WLC_{ox}^2 f} \left(\frac{G_M}{I_D} \right)^2 \quad (4)$$

In this way the parameter N_T can be determined. For $I_D > 100 \mu A$, the Coulomb scattering effect dominates and from equation (3), the α_C parameter can be extracted.

The whole procedure is shown in Fig. 4.3 [18]

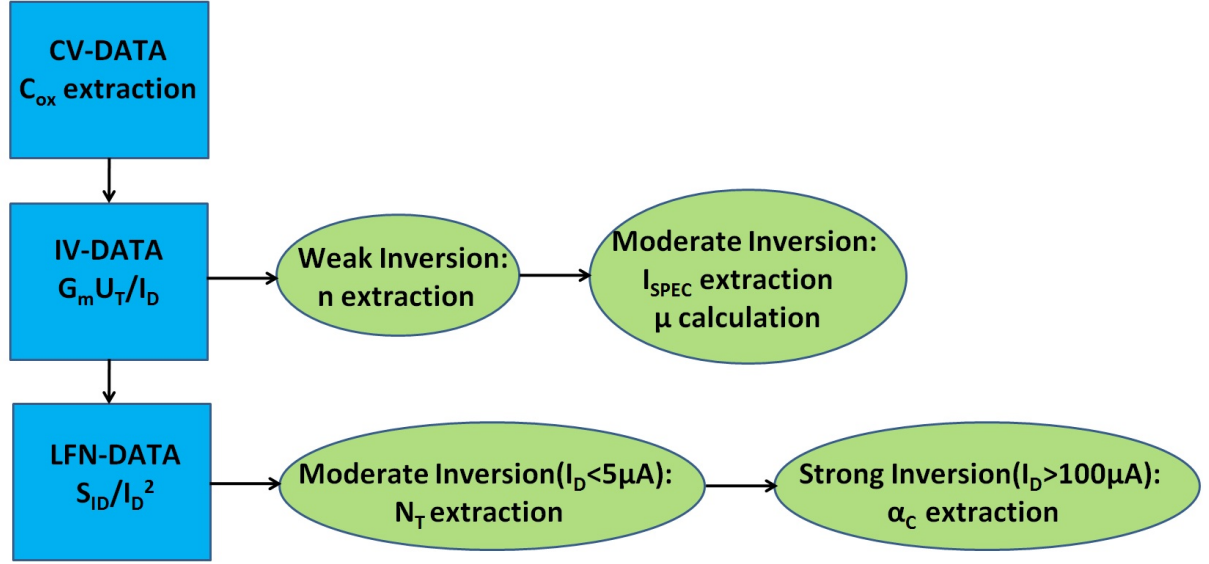


Figure 4.3 1/f noise parameter extraction flow chart[18]

4.2.1 Extracted parameters for N-channel devices 350nm

All the parameters that were extracted from IV and noise data, are shown in Table 4.1 for long and short N-channel devices.

PARAMETER	SYMBOL	UNITS	NMOS 40x10	NMOS 40x05
n	n	-	1.67	1.68
I _{spec}	I _{spec}	-	1.4 10 ⁻⁶	20 10 ⁻⁶
μ	μ _{eff}	cm ² (Vs) ⁻¹	740	1230
N _T	N _t	eV ⁻¹ cm ⁻³	1.62 10 ¹⁶	2.7 10 ¹⁶
AC	α _c	VsC ⁻¹	3 10 ³	6 10 ³

Table 4.1 Extracted parameters for long and short N-channel devices

At the end of this procedure, we calculate our simulated-data using the parameter extraction model equations, for both long and short N-channel devices.

NMOS 40x0.5

$$W = 40 \times 10^{-6} m, L = 500 \times 10^{-9} m, C_{ox} = 0.0023, g_m = 2.31 \times 10^{-5}, q_e = 1.6022 \times 10^{-19} C$$

$$N_{ST} = N_T \lambda_\lambda, \lambda_\lambda = 0.1 \times 10^{-9}, I_d = 1 \times 10^{-6}, \left(\frac{S_{ID}}{ID^2} \right)_{\Delta n} = 4.324 \times 10^{-9}, T = 297 K$$

$$K = 1.381 \times 10^{-23} m^2 kg s^{-2} K^{-1}$$

$$g_m = \frac{g_{ms}}{n} = \frac{g_m n U_T}{I_D} \quad 1 = 0.5933 n \Rightarrow n = \frac{1}{0.5933} \Rightarrow n_{NMOS40x0.5} = 1.6855$$

$$I_{SPEC} = 0.618 \frac{g_m}{I_{D_{MAX}}} \quad I_{spec} = 30 \times 10^{-6}, I_{spec} = 2n U_T^2 \mu C_{OX} \left(\frac{W}{DL+L} \right), \mu = \frac{I_{spec}(L+DL)}{2n U_T^2 C_{OX} W}$$

$$I_{spec} = 30 \times 10^{-6}, I_{spec} = 2n U_T^2 \mu C_{OX} \left(\frac{W}{DL+L} \right), \mu = \frac{I_{spec}(L+DL)}{2n U_T^2 C_{OX} W}$$

$$\mu = \frac{I_{spec}(L+DL)}{2n U_T^2 C_{OX} W} = \frac{30 \times 10^{-6} \times 0.681 \times 10^{-6}}{2 \times 1.6855 \times 0.00256^2 \times 0.0023 \times 40 \times 10^{-6}} \Rightarrow \mu_{NMOS40 \times 0.5} = 0.1009$$

$$\left(\frac{S_{ID}}{ID^2} \right)_{\Delta n} = \frac{g_m^2 K T q_e^2 N_{ST}}{I_D^2 W (L+DL) C_{OX}^2 f} \Rightarrow N_T \lambda_\lambda = \frac{I_D^2 W (L+DL) C_{OX}^2 f}{g_m^2 K T q_e^2} \left(\frac{S_{ID}}{ID^2} \right)_{\Delta n}$$

$$N_T = \frac{I_D^2 W (L+DL) C_{OX}^2 f}{g_m^2 K T q_e^2 \lambda_\lambda} \left(\frac{S_{ID}}{ID^2} \right)_{\Delta n} = \frac{(1 \times 10^{-6})^2 40 \times 10^{-6} 0.681 \times 10^{-6} 0.0023^2 4.324 \times 10^{-9}}{2.31 \times 10^{-5} 1.381 \times 10^{-23} 297 (1.6022 \times 10^{-19})^2 0.1 \times 10^{-9}}$$

$$N_{TNMOS40 \times 0.5} = \frac{1.109 \times 10^{41}}{1.6 \times 10^{25}} = 6.9314 \times 10^{15}$$

$$N_{TDATA} = 1.17 \times 10^{16}$$

NMOS 40x10

$$W = 40 \times 10^{-6} m, L = 10 \times 10^{-6} m, C_{OX} = 0.0023, q_e = 1.6022 \times 10^{-19} C, I_d = 1 \times 10^{-6}$$

$$N_{ST} = N_T \lambda_\lambda, \lambda_\lambda = 0.1 \times 10^{-9} m, g_m = 1.89 \times 10^{-5}, \left(\frac{S_{ID}}{ID^2} \right)_{\Delta n} = 3.174 \times 10^{-10}, T = 297 K$$

$$K = 1.381 \times 10^{-23} m^2 kg s^{-2} K^{-1}$$

$$g_m = \frac{g_{ms}}{n} = \frac{g_m n U_T}{I_D} \quad 1 = 0.5951 n \Rightarrow n = \frac{1}{0.5951} \Rightarrow n_{NMOS40 \times 10} = 1.68$$

$$I_{SPEC} = 0.618 \frac{g_m}{I_{D_{MAX}}}$$

$$I_{spec} = 1.4 \times 10^{-6}, I_{spec} = 2n U_T^2 \mu C_{OX} \left(\frac{W}{DL+L} \right), \mu = \frac{I_{spec}(L+DL)}{2n U_T^2 C_{OX} W}$$

$$\mu = \frac{I_{spec}(L+DL)}{2n U_T^2 C_{OX} W} = \frac{1.4 \times 10^{-6} \times 10.181 \times 10^{-6}}{2 \times 1.6855 \times 0.00256^2 \times 0.0023 \times 40 \times 10^{-6}} \Rightarrow \mu_{NMOS40 \times 10} = 0.0704$$

$$\left(\frac{S_{ID}}{ID^2} \right)_{\Delta n} = \frac{g_m^2 K T q_e^2 N_{ST}}{I_D^2 W (L+DL) C_{OX}^2 f} \Rightarrow N_T \lambda_\lambda = \frac{I_D^2 W (L+DL) C_{OX}^2 f}{g_m^2 K T q_e^2} \left(\frac{S_{ID}}{ID^2} \right)_{\Delta n}$$

$$N_T = \frac{I_D^2 W (L+DL) C_{OX}^2 f}{g_m^2 K T q_e^2 \lambda_\lambda} \left(\frac{S_{ID}}{ID^2} \right)_{\Delta n} = \frac{(1 \times 10^{-6})^2 40 \times 10^{-6} 10.181 \times 10^{-6} 0.0023^2 3.174 \times 10^{-10}}{1.89 \times 10^{-5} 1.381 \times 10^{-23} 297 (1.6022 \times 10^{-19})^2 0.1 \times 10^{-9}}$$

$$N_{TNMOS40 \times 10} = \frac{1.818 \times 10^{41}}{1.6 \times 10^{25}} = 1.1362 \times 10^{16}$$

$$N_{TDATA} = 1.17 \times 10^{16}$$

4.2.2 Extracted parameters for P-channel devices 350nm

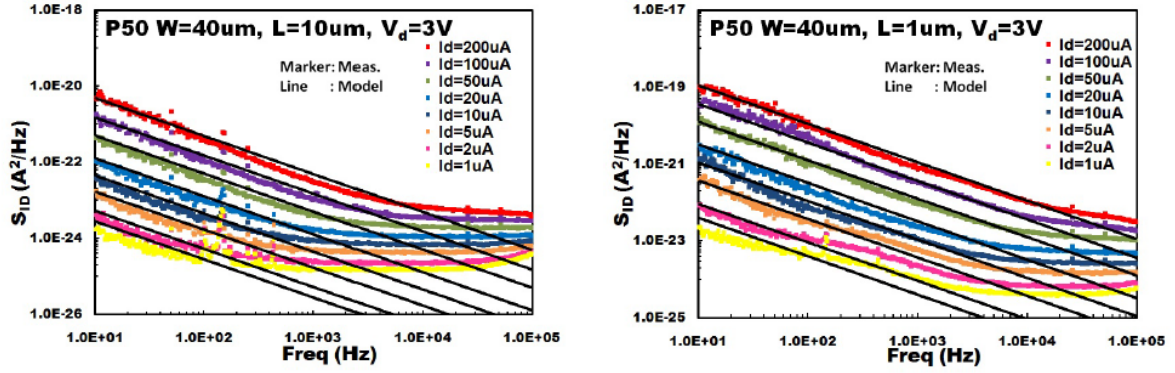


Fig. 4.4 - Power spectral density of drain current noise S_{ID} for 50 V long and short P-channel HV-MOSFETs, at $V_D = 3$ V for 8 different I_D values from 1 μ A to 200 μ A.

All the parameters that were extracted from IV and noise data, are shown in Table 4.2 for long and short P-channel devices.

PARAMETER	SYMBOL	UNITS	PMOS 40x10	PMOS 40x1
n	n	-	1.67	1.68
I _{spec}	I _{spec}	-	1.4 10 ⁻⁶	20 10 ⁻⁶
μ	μ_{eff}	cm ² (Vs) ⁻¹	740	1230
NT	N _t	eV ⁻¹ cm ⁻³	1.62 10 ¹⁶	2.7 10 ¹⁶
AC	α_c	VsC ⁻¹	3 10 ³	6 10 ³

Table 4.1 Extracted parameters for long and short N-channel devices

PMOS 40x1

$$W = 40 \times 10^{-6} \text{ m}, L = 1 \times 10^{-6} \text{ m}, C_{OX} = 0.0023, g_m = 2.832 \times 10^{-5}, q_e = 1.6022 \times 10^{-19} \text{ C}$$

$$N_{ST} = N_T \lambda_\lambda, \lambda_\lambda = 0.1 \times 10^{-9}, I_d = 1 \times 10^{-6}, \left(\frac{S_{ID}}{I_D^2} \right)_{\Delta n} = 2.767 \times 10^{-10}, T = 297 \text{ K}$$

$$K = 1.381 \times 10^{-23} \text{ m}^2 \text{ kg s}^{-2} \text{ K}^{-1}$$

$$g_m = \frac{g_{ms}}{n} = \frac{g_m n U_T}{I_D} \quad 1 = 0.7247 n \Rightarrow n = \frac{1}{0.7247} \Rightarrow n_{PMOS40x1} = 1.3799$$

$$I_{SPEC} = 0.618 \frac{g_m}{I_{DMAX}} \quad I_{spec} = 2.961 \times 10^{-6}, I_{spec} = 2n U_T^2 \mu C_{OX} \left(\frac{W}{DL + L} \right), \mu = \frac{I_{spec} (L + DL)}{2n U_T^2 C_{OX} W}$$

$$\mu = \frac{I_{spec} (L + DL)}{2n U_T^2 C_{OX} W} = \frac{2.961 \times 10^{-6} \times 1.101 \times 10^{-6}}{2 \times 1.3799 \times 0.00256^2 \times 0.0023 \times 40 \times 10^{-6}} \Rightarrow \mu_{PMOS40x1} = 0.0196$$

$$\left(\frac{S_{ID}}{ID^2}\right)_{\Delta n} = \frac{g_m^2 KT q_e^2 N_{ST}}{I_D^2 W (L+ DL) C_{OX}^2 f} \Rightarrow N_T \lambda_\lambda = \frac{I_D^2 W (L+ DL) C_{OX}^2 f}{g_m^2 KT q_e^2} \left(\frac{S_{ID}}{ID^2}\right)_{\Delta n}$$

$$N_T = \frac{I_D^2 W (L+ DL) C_{OX}^2 f}{g_m^2 KT q_e^2 \lambda_\lambda} \left(\frac{S_{ID}}{ID^2}\right)_{\Delta n} = \frac{(1 \times 10^{-6})^2 40 \times 10^{-6} 1.101 \times 10^{-6} 0.0023^2 2.767 \times 10^{-10}}{2.832 \times 10^{-5} 1.381 \times 10^{-23} 297 (1.6022 \times 10^{-19})^2 0.1 \times 10^{-9}}$$

$$N_{TPMOS40x1} = \frac{7.6338 \times 10^{39}}{1.6 \times 10^{25}} = 4.7711 \times 10^{14}$$

$$N_{TDATA} = 1.17 \times 10^{16}$$

PMOS 40x10

$$W = 40 \times 10^{-6} m, L = 10 \times 10^{-6} m, C_{OX} = 0.0023, g_m = 1.531 \times 10^{-5}, q_e = 1.6022 \times 10^{-19} C$$

$$N_{ST} = N_T \lambda_\lambda, \lambda_\lambda = 0.1 \times 10^{-9}, I_d = 1 \times 10^{-6}, \left(\frac{S_{ID}}{ID^2}\right)_{\Delta n} = 1.988 \times 10^{-11}, T = 297 K$$

$$K = 1.381 \times 10^{-23} m^2 kg s^{-2} K^{-1}$$

$$g_m = \frac{g_{ms}}{n} = \frac{g_m n U_T}{I_D} \quad 1 = 0.7298 n \Rightarrow n = \frac{1}{0.7298} \Rightarrow n_{PMOS40x10} = 1.3702$$

$$I_{SPEC} = 0.618 \frac{g_m}{I_{DMAX}}$$

$$I_{spec} = 300 \times 10^{-9}, I_{spec} = 2n U_T^2 \mu C_{OX} \left(\frac{W}{DL+ L}\right), \mu = \frac{I_{spec} (L+ DL)}{2n U_T^2 C_{OX} W}$$

$$\mu = \frac{I_{spec} (L+ DL)}{2n U_T^2 C_{OX} W} = \frac{300 \times 10^{-9} \times 10.101 \times 10^{-6}}{2 \times 1.3722 \times 0.00256^2 \times 0.0023 \times 40 \times 10^{-6}} \Rightarrow \mu_{PMOS40x10} = 0.0183$$

$$\left(\frac{S_{ID}}{ID^2}\right)_{\Delta n} = \frac{g_m^2 KT q_e^2 N_{ST}}{I_D^2 W (L+ DL) C_{OX}^2 f} \Rightarrow N_T \lambda_\lambda = \frac{I_D^2 W (L+ DL) C_{OX}^2 f}{g_m^2 KT q_e^2} \left(\frac{S_{ID}}{ID^2}\right)_{\Delta n}$$

$$N_T = \frac{I_D^2 W (L+ DL) C_{OX}^2 f}{g_m^2 KT q_e^2 \lambda_\lambda} \left(\frac{S_{ID}}{ID^2}\right)_{\Delta n} = \frac{(1 \times 10^{-6})^2 40 \times 10^{-6} 10.101 \times 10^{-6} 0.0023^2 1.988 \times 10^{-11}}{1.531 \times 10^{-5} 1.381 \times 10^{-23} 297 (1.6022 \times 10^{-19})^2 0.1 \times 10^{-9}}$$

$$N_{TPMOS40x10} = \frac{1.7217 \times 10^{40}}{1.6 \times 10^{25}} = 1.0761 \times 10^{15}$$

$$N_{TDATA} = 1.16 \times 10^{15}$$

4.2.3 Bias dependence analysis of 1/f noise - Model validation

Modelling results are shown in Fig. 4.5 and 4.6 both for long (a) and short (b) N-P channel devices. Output noise, divided by I_D^2 , as well as input noise $S_{VG} = S_{ID}/G_M^2$ versus I_D are shown. In each case, the complete model is represented by a thick line and the model without the Coulomb scattering effect ($\alpha\mu=0$) is represented by a dashed line. It is clear that these two lines almost coincide in moderate inversion regime which means that indeed in this region the Coulomb scattering effect on noise is negligible[18].

-NMOS 350nm W=40um L=10um/500nm

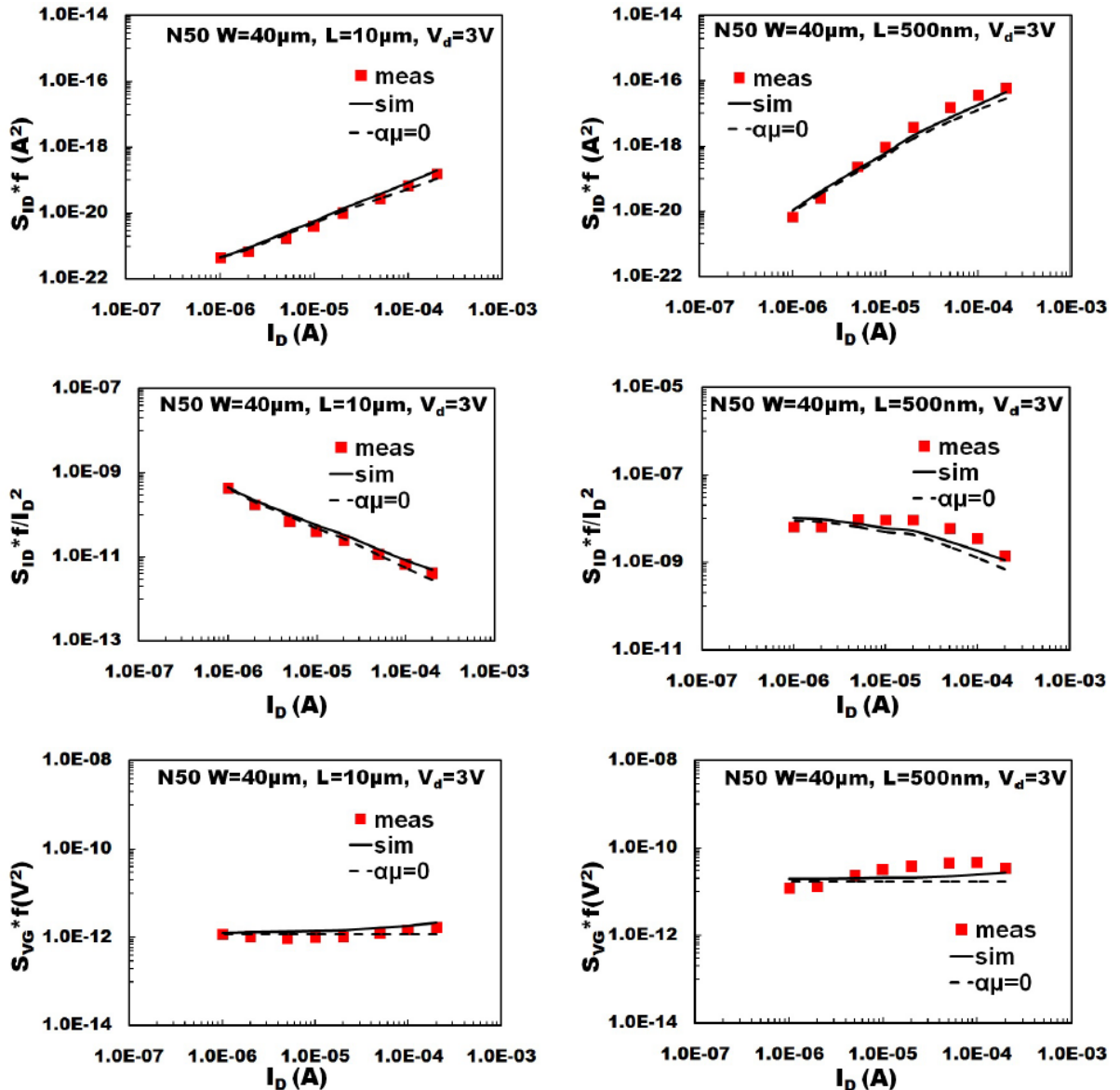


Fig 4.5 Low frequency noise PSD S_{ID} , S_{ID}/I_D^2 and S_{VG} , referred to 1 Hz, vs. drain current I_D , for 50V transistors. a) Long device ($W = 40 \mu\text{m}$, $L = 10 \mu\text{m}$). b) Short device ($W = 40 \mu\text{m}$, $L = 500 \text{nm}$); measurement (markers) and model (lines)

-PMOS 350nm W=40um L=10um/1um

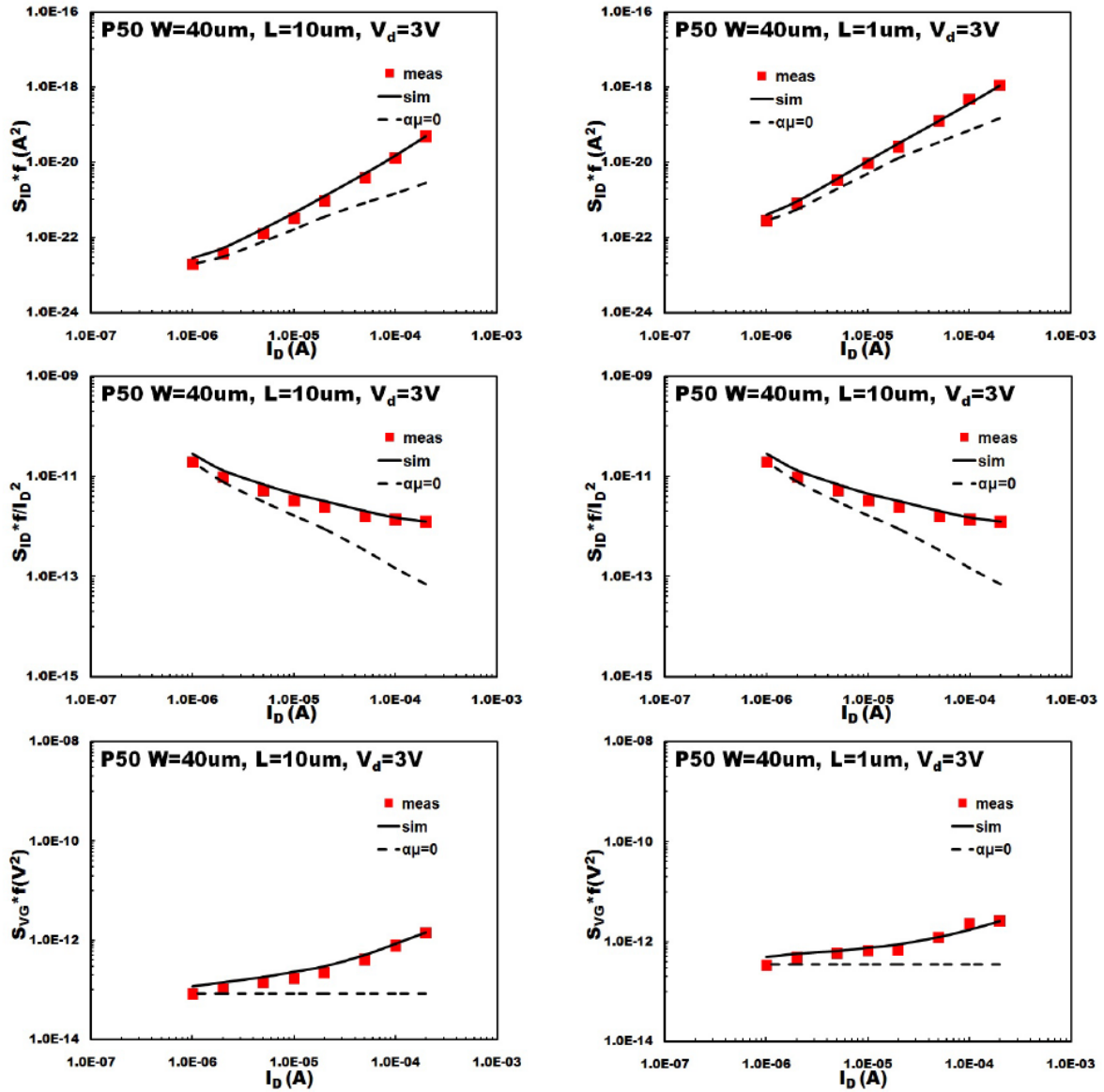


Fig 4.6 Low frequency noise PSD S_{ID} , S_{ID}/I_D^2 and S_{VG} , referred to 1 Hz, vs. drain current I_D , for P50 transistors. a) Long device ($W = 40 \mu\text{m}$, $L = 10 \mu\text{m}$). b) Short device ($W = 40 \mu\text{m}$, $L = 1 \mu\text{m}$); measurement (markers) and model (lines).

We also validate our measurements with other model. Results are shown in Fig. 4.7 both for long (a) and short (b) N-P channel devices. Output noise, output noise divided by I_D^2 , as well as input noise $S_{VG} = S_{ID}/G_M^2$ versus I_D are shown. In each case, the complete model is represented by a thick line, simple model is represented by dashed line and measurements are represented by markers. In general results are good.

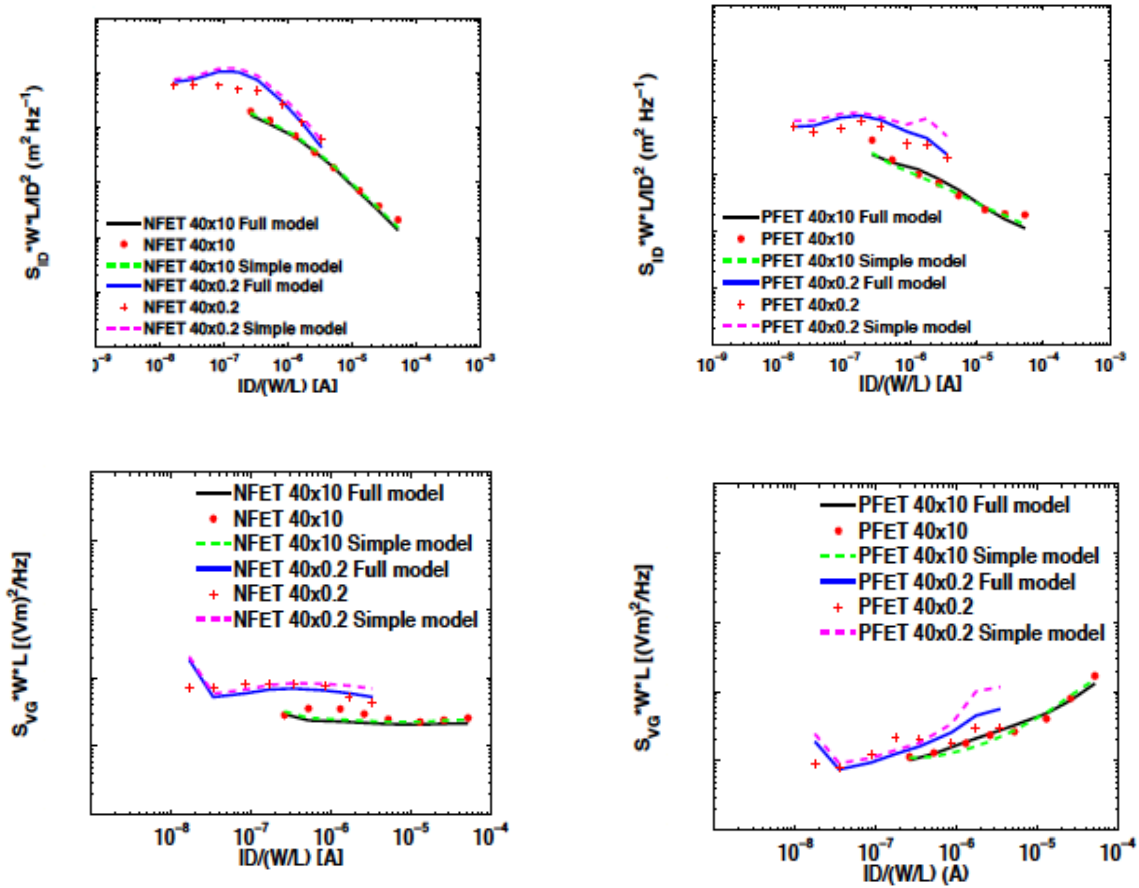


Fig 4.7 Low frequency noise PSD S_{ID} , $S_{ID} * W * L$ and $S_{VG} * W * L$, referred to 1 Hz, vs. drain current $I_D/(W/L)$, for P50 transistors. a) Long device ($W = 40 \mu m$, $L = 10 \mu m$). b) Short device ($W = 40 \mu m$, $L = 200 nm$); measurement (markers) and models (lines).

Chapter 5: Results and discussion

The spectral dependence of LFN is considered here to be reasonably close to $1/f$. Of course things are somewhat more complicated [8], but this formula can be considered sufficient for a first evaluation of LFN parameters.

Generally speaking, the model shows a very consistent behavior especially for long N-channel devices. For the short device, results are not perfect due to the limited current range for the extraction of the parameter α_C . For such a device, the highest level of measured current ($I_D = 200 \mu\text{A}$) is just slightly above the onset of strong inversion. On the other hand, the decrease of noise observed in S_{VG} for the same short-channel device at lower currents may be regarded as non-typical, and is actually a result of the slight departure from $1/f$ in the noise spectra of the short-channel device.

The extracted $1/f$ noise parameters, together with the auxiliary electrical parameters, are obtained individually for long and short devices. Ideally, the measurement of devices of intermediate channel lengths would provide a more complete picture of channel-length dependence.

However, we note that the $1/f$ noise parameters for the long- and short-channel devices are reasonably close. A scalable model valid for all channel lengths is highly desirable; therefore, in practice, a single noise parameter set might be chosen to cover all devices, incurring a slight loss of accuracy.

APPENDIX A

We provide the matlab code that help us to calculate gate voltage noise and validate Simple Model compare to other Full Models.

```
clc
clear all
close all

data = importdata('/Users/cfellas/Desktop/Measurements/H35_COMON_DEVICES/COMON
MEASUREMENTS/ADMOS/NOISE/NMOS50M/40x0.5/40_0.5_300av_3V_11.txt',' ');
freq=data(9:409,1); %frequency
id_200=data(9:409,2);% id 200uA
id_100=data(9:409,3);% id 100uA
id_50=data(9:409,4);% id 50uA
id_20=data(9:409,5);% id 20uA
id_10=data(9:409,6);% id 10uA
id_5=data(9:409,7);% id 5uA
id_2=data(9:409,8);% id 2uA
id_1=data(9:409,9);% id 1uA
vg1st=data(1,2:9);
id1st=data(4,2:9);

% figure(1)
% loglog(freq,id_200,'r-',freq,id_100,'g-',freq,id_50,'b-',freq,id_20,'c-',freq,id_10,'m-',freq,id_5,'y-
',freq,id_2,'k-',freq,id_1,'b--')
% grid on;
% ylabel('id [A]');
% xlabel('Frequency [Hz]');
% title('1st measuremnet NMOS50M 40x0.5 id vs Freequency for all id ');
% legend('id[200uA]','id[100uA]','id[50uA]','id[20uA]','id[10uA]','id[5uA]','id[2uA]','id[1uA]')
% axis([ 10e01 10e04 10e-14 10e-10 ])
%
%
% figure(2)
% plot(abs(vg1st),id1st)
% grid on;
% ylabel('id [A]');
% xlabel('Vg [V]');
% title('1st measuremnet NMOS50M 40x0.5 id vs Vg ');
% set(gca,'YTickLabel',num2str(get(gca,'YTick')));
% set(gca,'XTickLabel',num2str(get(gca,'XTick')));

data_1 =importdata('/Users/cfellas/Desktop/Measurements/H35_COMON_DEVICES/COMON
MEASUREMENTS/ADMOS/NOISE/NMOS50M/40x0.5/40_0.5_300av_3V_12.txt',' ');
freq_1=data_1(9:409,1); %frequency
```

```

id_100_1=data_1(9:409,3);% id 100uA
id_50_1=data_1(9:409,4);% id 50uA
id_20_1=data_1(9:409,5);% id 20uA
id_10_1=data_1(9:409,6);% id 10uA
id_5_1=data_1(9:409,7);% id 5uA
id_2_1=data_1(9:409,8);% id 2uA
id_1_1=data_1(9:409,9);% id 1uA
vg2nd=data_1(1,2:9);
id2nd=data_1(4,2:9);

% figure(3)
% loglog(freq,id_200_1,'r-',freq,id_100_1,'g-',freq,id_50_1,'b-',freq,id_20_1,'c-',freq,id_10_1,'m-
',freq,id_5_1,'y-',freq,id_2_1,'k-',freq,id_1_1,'b--')
% grid on;
% ylabel('id [A]');
% xlabel('Frequency [Hz]');
% title('2nd measuremnet NMOS50M 40x0.5 id vs Freequency for all id ');
% legend('id[200uA]','id[100uA]','id[50uA]','id[20uA]','id[10uA]','id[5uA]','id[2uA]','id[1uA]')
% axis([ 10e01 10e04 10e-14 10e-10 ])
%
%
% figure(4)
% plot(abs(vg2nd),id2nd)
% grid on;
% ylabel('id [A]');
% xlabel('Vg [V]');
% title('2nd measuremnet NMOS50M 40x0.5 id vs Vg ');
% set(gca,'YTickLabel',num2str(get(gca,'YTick')));
% set(gca,'XTickLabel',num2str(get(gca,'XTick')));

data_2=importdata('/Users/cfellas/Desktop/Measurements/H35_COMON_DEVICES/COMON
MEASUREMENTS/ADMOS/NOISE/NMOS50M/40x0.5/40_0.5_300av_3V_13.txt','');
freq_2=data_2(9:409,1); %frequency
id_200_2=data_2(9:409,2);% id 200uA
id_100_2=data_2(9:409,3);% id 100uA
id_50_2=data_2(9:409,4);% id 50uA
id_20_2=data_2(9:409,5);% id 20uA
id_10_2=data_2(9:409,6);% id 10uA
id_5_2=data_2(9:409,7);% id 5uA
id_2_2=data_2(9:409,8);% id 2uA
id_1_2=data_2(9:409,9);% id 1uA
vg3rd=data_2(1,2:9);
id3rd=data_2(4,2:9);

% figure(5)
% loglog(freq,id_200_2,'r-',freq,id_100_2,'g-',freq,id_50_2,'b-',freq,id_20_2,'c-',freq,id_10_2,'m-
',freq,id_5_2,'y-',freq,id_2_2,'k-',freq,id_1_2,'b--')
% grid on;
% ylabel('id [A]');
% xlabel('Frequency [Hz]');
% title('3rd measuremnet NMOS50M 40x0.5 id vs Freequency for all id ');
% legend('id[200uA]','id[100uA]','id[50uA]','id[20uA]','id[10uA]','id[5uA]','id[2uA]','id[1uA]')

```

```

%
%
% figure(6)
% plot(abs(vg3rd),id3rd)
% grid on;
% ylabel('id [A]');
% xlabel('Vg [V]');
% title('3rd measuremnet NMOS50M 40x0.5 id vs Vg ');
% set(gca,'YTickLabel',num2str(get(gca,'YTick')));
% set(gca,'XTickLabel',num2str(get(gca,'XTick')));

data_3=importdata('/Users/cfellas/Desktop/Measurements/H35_COMON_DEVICES/COMON
MEASUREMENTS/ADMOS/NOISE/NMOS50M/40x0.5/40_0.5_300av_3V_14.txt',' ');
freq_3=data_3(9:409,1); %frequency
id_200_3=data_3(9:409,2);% id 200uA
id_100_3=data_3(9:409,3);% id 100uA
id_50_3=data_3(9:409,4);% id 50uA
id_20_3=data_3(9:409,5);% id 20uA
id_10_3=data_3(9:409,6);% id 10uA
id_5_3=data_3(9:409,7);% id 5uA
id_2_3=data_3(9:409,8);% id 2uA
id_1_3=data_3(9:409,9);% id 1uA
vg4th=data_3(1,2:9);
id4th=data_3(4,2:9);%
%
% figure(7)
% loglog(freq,id_200_3,'r-',freq,id_100_3,'g-',freq,id_50_3,'b-',freq,id_20_3,'c-',freq,id_10_3,'m-
',freq,id_5_3,'y-',freq,id_2_3,'k-',freq,id_1_3,'b--')
% grid on;
% ylabel('id [A]');
% xlabel('Frequency [Hz]');
% title('4th measuremnet NMOS50M 40x0.5 id vs Freequency for all id ');
% legend('id[200uA]','id[100uA]','id[50uA]','id[20uA]','id[10uA]','id[5uA]','id[2uA]','id[1uA]')
% axis([ 10e01 10e04 10e-14 10e-10 ])
%
% figure(8)
% plot(abs(vg4th),id4th)
% grid on;
% ylabel('id [A]');
% xlabel('Vg [V]');
% title('4th measuremnet NMOS50M 40x0.5 id vs Vg ');
% set(gca,'YTickLabel',num2str(get(gca,'YTick')));
% set(gca,'XTickLabel',num2str(get(gca,'XTick')));
%

data_4=importdata('/Users/cfellas/Desktop/Measurements/H35_COMON_DEVICES/COMON
MEASUREMENTS/ADMOS/NOISE/NMOS50M/40x0.5/40_0.5_300av_3V_15.txt',' ');
freq_4=data_4(9:409,1); %frequency
id_200_4=data_4(9:409,2);% id 200uA
id_100_4=data_4(9:409,3);% id 100uA
id_50_4=data_4(9:409,4);% id 50uA

```

```

id_10_4=data_4(9:409,6);% id 10uA
id_5_4=data_4(9:409,7);% id 5uA
id_2_4=data_4(9:409,8);% id 2uA
id_1_4=data_4(9:409,9);% id 1uA
vg5th=data_4(1,2:9);
id5th=data_4(4,2:9);

% figure(9)
% loglog(freq,id_200_4,'r-',freq,id_100_4,'g-',freq,id_50_4,'b-',freq,id_20_4,'c-',freq,id_10_4,'m-
',freq,id_5_4,'y-',freq,id_2_4,'k-',freq,id_1_4,'b--')
% grid on;
% ylabel('id [A]');
% xlabel('Frequency [Hz]');
% title('5th measuremnet NMOS50M 40x0.5 id vs Freequency for all id ');
% legend('id[200uA]','id[100uA]','id[50uA]','id[20uA]','id[10uA]','id[5uA]','id[2uA]','id[1uA]')
% axis([ 10e01 10e04 10e-14 10e-10 ])
%
% figure(10)
% plot(abs(vg5th),id5th)
% grid on;
% ylabel('id [A]');
% xlabel('Vg [V]');
% title('5th measuremnet NMOS50M 40x0.5 id vs Vg ');
% set(gca,'YTickLabel',num2str(get(gca,'YTick')));
% set(gca,'XTickLabel',num2str(get(gca,'XTick')));

```

```

%%%%%%%% Mean of Frequency ,vg,id

```

```

freqs=[freq freq_1 freq_2 freq_3 freq_4];
freq_40_05=zeros((length(freqs)),1);

```

```

for i=1:length(freqs)
    freq_40_05(i,1)=mean(freqs(i,:));
end

```

```

vgs=[vg1st;vg2nd;vg3rd;vg4th;vg5th;];

```

```

vg_NMOS40_05=mean(vgs);
save vg_NMOS40_05.txt -ascii vg_NMOS40_05

```

```

ids=[id1st;id2nd;id3rd;id4th;id5th;];

```

```

id_40_05=mean(ids);
save id_NMOS40_05.txt -ascii id_NMOS40_05

```

```

-----

```

```

a=[id_200 id_200_1 id_200_2 id_200_3 id_200_4];
id200_40_05=zeros((length(a)+1),3);

for i=1:length(a)
    id200_40_05(i,2)=mean(a(i,:));
    id200_40_05(i,1)=(freq_40_05(i,:));
    id200_40_05((length(a)+1),1)=0;

end
%
% % save id200_40_05.txt -ascii id200_40_05
%
b=[id_100 id_100_1 id_100_2 id_100_3 id_100_4];
id100_40_05=zeros((length(b)+1),3);

for i=1:length(b)
    id100_40_05(i,2)=mean(b(i,:));
    id100_40_05(i,1)=(freq_40_05(i,:));
    id100_40_05((length(b)+1),1)=0;
end
%
% % save id100_40_05.txt -ascii id100_40_05
% %
% %
%
c=[id_50 id_50_1 id_50_2 id_50_3 id_50_4];
id50_40_05=zeros((length(c)+1),3);

for i=1:length(c)
    id50_40_05(i,2)=mean(c(i,:));
    id50_40_05(i,1)=(freq_40_05(i,:));
    id50_40_05((length(c)+1),1)=0;
end
%
% % save id50_40_05.txt -ascii id50_40_05
% %
% %
d=[id_20 id_20_1 id_20_2 id_20_3 id_20_4];
id20_40_05=zeros((length(d)+1),3);

for i=1:length(d)
    id20_40_05(i,2)=mean(d(i,:));
    id20_40_05(i,1)=(freq_40_05(i,:));
    id20_40_05((length(d)+1),1)=0;
end
%
% % save id20_40_05.txt -ascii id20_40_05
% %
% %
e=[id_10 id_10_1 id_10_2 id_10_3 id_10_4];
id10_40_05=zeros((length(e)+1),3);

```

```

    id10_40_05(i,2)=mean(e(i,:));
    id10_40_05(i,1)=(freq_40_05(i,:));
    id10_40_05((length(e)+1),1)=0;
end
% %
% % save id10_40_05.txt -ascii id10_40_05
% %
% %
f=[id_5 id_5_1 id_5_2 id_5_3 id_5_4];
id5_40_05=zeros((length(f)+1),3);

for i=1:length(f)
    id5_40_05(i,2)=mean(f(i,:));
    id5_40_05(i,1)=(freq_40_05(i,:));
    id5_40_05((length(f)+1),1)=0;
end
%
% % save id5_40_05.txt -ascii id5_40_05
% %
% %
g=[id_2 id_2_1 id_2_2 id_2_3 id_2_4];
id2_40_05=zeros((length(g)+1),3);

for i=1:length(g)
    id2_40_05(i,2)=mean(g(i,:));
    id2_40_05(i,1)=(freq_40_05(i,:));
    id2_40_05((length(g)+1),1)=0;
end
% %
% % save id2_40_05.txt -ascii id2_40_05
% %
h=[id_1 id_1_1 id_1_2 id_1_3 id_1_4];
id1_40_05=zeros((length(h)+1),3);

for i=1:length(h)
    id1_40_05(i,2)=mean(h(i,:));
    id1_40_05(i,1)=(freq_40_05(i,:));
    id1_40_05((length(h)+1),1)=0;
end
% %
%
NMOS50M140_05=[id200_40_05;id100_40_05;id50_40_05;id20_40_05;id10_40_05;id5_40_05;id2_40_05;id1_40_05];
save NMOS50M140_05.txt -ascii NMOS50M140_05

% %%% Mesos oros metrisewn
%
%
% % figure(11)
% loglog(freq,id_200,'k-',freq,id_200_1,'k-',freq,id_200_2,'k-',freq,id_200_3,'k-',freq,id_200_4,'k-
','freq,id200_40_05','r*')
% grid on;
% ylabel('id [A]');
% xlabel('Frequency [Hz]');

```

```

% legend('id[200]1','id[200]2','id[200]3','id[200]4','id[200]5','id200_40_05')
% axis([ 10e01 10e04 10e-13 10e-08 ])
%
% figure(12)
% loglog(freq,id_100,'k-',freq,id_100_1,'k-',freq,id_100_2,'k-',freq,id_100_3,'k-',freq,id_100_4,'k-
',freq,id100_40_05,'r*')
% grid on;
% ylabel('id [A]');
% xlabel('Frequency [Hz]');
% title('All measuremnets for NMOS50M 40x0.5 id[100uA] vs Freequency');
% legend('id[100]1','id[100]2','id[100]3','id[100]4','id[100]5','id100_40_05')
% axis([ 10e01 10e04 10e-13 10e-08 ])
%
%
% figure(13)
% loglog(freq,id_50,'k-',freq,id_50_1,'k-',freq,id_50_2,'k-',freq,id_50_3,'k-',freq,id_50_4,'k-
',freq,id50_40_05,'r*')
% grid on;
% ylabel('id [A]');
% xlabel('Frequency [Hz]');
% title('All measuremnets for NMOS50M 40x0.5 id[50uA] vs Freequency');
% legend('id[50]1','id[50]2','id[50]3','id[50]4','id[50]5','id50_40_05')
% axis([ 10e01 10e04 10e-13 10e-08 ])
%
%
% figure(14)
% loglog(freq,id_20,'k-',freq,id_20_1,'k-',freq,id_20_2,'k-',freq,id_20_3,'k-',freq,id_20_4,'k-
',freq,id20_40_05,'r*')
% grid on;
% ylabel('id [A]');
% xlabel('Frequency [Hz]');
% title('All measuremnets for NMOS50M 40x0.5 id[20uA] vs Freequency');
% legend('id[20]1','id[20]2','id[20]3','id[20]4','id[20]5','id20_40_05')
% axis([ 10e01 10e04 10e-13 10e-08 ])
%
%
% figure(15)
% loglog(freq,id_10,'k-',freq,id_10_1,'k-',freq,id_10_2,'k-',freq,id_10_3,'k-',freq,id_10_4,'k-
',freq,id10_40_05,'r*')
% grid on;
% ylabel('id [A]');
% xlabel('Frequency [Hz]');
% title('All measuremnets for NMOS50M 40x0.5 id[10uA] vs Freequency');
% legend('id[10]1','id[10]2','id[10]3','id[10]4','id[10]5','id10_40_05')
% axis([ 10e01 10e04 10e-13 10e-08 ])
%
%
% figure(16)
% loglog(freq,id_5,'k-',freq,id_5_1,'k-',freq,id_5_2,'k-',freq,id_5_3,'k-',freq,id_5_4,'k-
',freq,id5_40_05,'r*')
% grid on;
% ylabel('id [A]');
% xlabel('Frequency [Hz]');
% title('All measuremnets for NMOS50M 40x0.5 id[5uA] vs Freequency');

```



```

% axis([ 10e01 10e04 10e-14 10e-10 ])
%
%
% figure(17)
% loglog(freq,id_2,'k-',freq,id_2_1,'k-',freq,id_2_2,'k-',freq,id_2_3,'k-',freq,id_2_4,'k-
',freq,id2_40_05,'r*')
% grid on;
% ylabel('id [A]');
% xlabel('Frequency [Hz]');
% title('All measuremnets for NMOS50M 40x0.5 id[2uA] vs Freequency');
% legend('id[2]1','id[2]2','id[2]3','id[2]4','id[2]5','id2_40_05')
% axis([ 10e01 10e04 10e-14 10e-11 ])
%
%
% figure(18)
% loglog(freq,id_1,'k-',freq,id_1_1,'k-',freq,id_1_2,'k-',freq,id_1_3,'k-',freq,id_1_4,'k-
',freq,id1_40_05,'r*')
% grid on;
% ylabel('id [A]');
% xlabel('Frequency [Hz]');
% title('All measuremnets for NMOS50M 40x0.5 id[1uA] vs Freequency');
% legend('id[1]1','id[1]2','id[1]3','id[1]4','id[1]5','id1_40_05')
% axis([ 10e01 10e04 10e-14 10e-11 ])

```

References

- [1] <http://en.wikipedia.org/wiki/Noise>
- [2] Paul Lim, PHD Thesis "Low Frequency Noise as a Characterization and reliability tool for the evaluation of Advanced MOSFETs", September 2009, Stanford University
- [3] Y.S Chauchan "COMPACT MODELLING OF HIGH VOLTAGE MOSFETs" PHD THESIS, Lausanne, EPFL, 2007
- [4] Costin Anghel " High Voltage Devices for standard MOSFET technologies Characterization and Modelling, PHD thesis, Lausanne EPFL, 2004
- [5] A. Bazigos, F. Krummenacher, J.-M. Sallese, M. Bucher, E. Seebacher, W. Posch, K. Molnar, M. Tang, "A Physics-Based Analytical Compact Model for the Drift Region of the HV-MOSFET", *IEEE Trans. on Electron Devices*, vol. 58, no. 6, pp. 1710-1721, June 2011.
- [6] A. Bazigos, F. Krummenacher, J.-M. Sallese, M. Bucher, E. Seebacher, W. Posch, K. Molnar, M. Tang, "RF Compact Modeling of High-voltage MOSFETs," *IETE Journal of Research*, vol. 58, no. 3, pp. 214-221, May-June 2012.
- [7] Y. S. Chauhan, F. Krummenacher, R. Gillon, B. Bakeroort, M. J. Declercq, A. M. Ionescu, "Compact Modeling of Lateral Nonuniform Doping in High-Voltage MOSFETs", *IEEE Trans. on Electron Devices*, vol. 54, no. 6, pp. 1527-1539, June 2007.
- [8] N. Mavredakis, M. Bucher, R. Friedrich, A. Bazigos, F. Krummenacher, J.-M. Sallese, T. Gneiting, W. Pflanzl, E. Seebacher, "Measurements and Compact Modelling of 1/f Noise in HV-MOSFETs," *IEEE Trans. on Electron Devices*, vol. 60, no. 2, pp. 670-676, Feb. 2013.
- [9] A. Dikshit, V. Subramanian, S. Pandharpure, S. Sirohi, T. Letavic, "Influence of drift region on the 1/f noise in LDMOS", *Int. Symp. on Power Semiconductor Devices and ICs (ISPSD)*, pp. 315-318, Bruges, Belgium, 3-7 June 2012.
- [10] M. I. Mahmud, Z. Celik-Butler, P. Hao, P. Srinivasan, F. Hou, B. L. Amey, S. Pendharkar, "Effect of Stress-Induced Degradation in LDMOS 1/f Noise Characteristics," *IEEE Electron Device Lett.*, vol. 33, no. 1, pp. 107-109, Jan. 2012.
- [11] M. I. Mahmud, Z. Celik-Butler, P. Hao, P. Srinivasan, F. Hou, C. Xu, B. L. Amey, S. Pendharkar, "A Physics-Based Analytical 1/f Noise Model for RESURF LDMOS Transistors," *IEEE Trans. on Electron Devices*, vol. 60, no. 2, pp. 677-683, Feb. 2013.

- [12] C. Enz, E. Vittoz, "Charge Based MOS Transistor Modeling", John Wiley and Sons, Chichester, 2006.
- [13] A. L. McWhorter, "1/f noise and germanium surface properties", in *Semiconductor Surface Physics*, ed. R. H. Kingston (University of Pennsylvania Press), pp. 207-228, 1957.
- [14] R. Kolarova, T. Skotnicki, J.A. Chroboczek, "Low frequency noise in thin gate oxide MOSFETs," *Microelectronics Reliability*, vol. 41, pp. 579 – 585, Feb. 2001.
- [15] N. Mavredakis, A. Antonopoulos, M. Bucher, "Bias Dependence of Low Frequency Noise in 90nm CMOS", *Proc. NSTI-Nanotech/Microtech Conf.*, vol. 2, pp. 805-808, Anaheim, California, June 21-25, 2010.
- [16] N. Mavredakis, A. Antonopoulos, M. Bucher, "Measurement and Modeling of 1/f Noise in 180 nm NMOS and PMOS Devices", *Europ. Conf. on Circuits & Systems for Communications (ECCSC)*, pp. 86-89, Belgrade, Serbia, Nov. 23-25, 2010.
- [17] A. Bazigos, M. Bucher, J. Assenmacher, S. Decker, W. Grabinski, Y. Papananos, "An Adjusted Constant-Current Method to Determine Saturated and Linear Mode Threshold Voltage of MOSFETs", *IEEE Trans. on Electron Devices*, vol. 58, no. 11, pp. 3751-3758, Nov. 2011.
- [18] Konstantinos Fellas, Nikolaos Mavredakis, Walter Pflanzl, Ehrenfried Seebacher, and Matthias Bucher " Simple 1/f Noise Parameter Extraction Method for High-Voltage MOSFETs " IEEE, MIEL, Belgrade, 2014