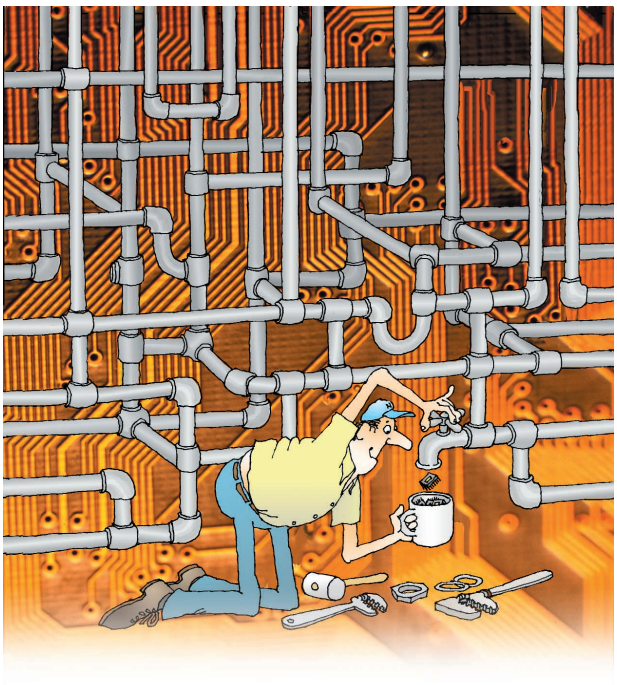

Guest Editors' Introduction

Network Processors for Future High-End Systems and Applications

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The rapid advancements of optical networking technology have increased the capacity of physical interconnection links to the point where you might consider bandwidth an always-available resource. This has shifted the bottleneck to the processing devices—routers and switches—demanding their gradual replacement with more sophisticated and powerful systems, tailored to the special characteristics of the supported multimedia streams.

As the global economy changes, time to market is becoming a dominant concern in the networking world. The networking and telecommunication industry, after a major market correction over the last four years, reveals solid signs of recovery. Nowadays, it is extremely important for manufacturers to present, in a timely fashion, innovative, well-defined, flexible, and low-cost products, which will diversify and distinguish them from the competition.

In this aggressive environment—both from the technology and market viewpoint—new semiconductor devices, called network processors (NPs), have emerged. We can define an NP as a highly integrated communications circuit, optimized to provide programmable processing of protocol data units (PDUs) at high speed (preferably at wire speed). Although programmability is a key factor for an NP, it might also accommodate hardwired components, dedicated to perform well-defined tasks that rarely change over time (for example, framing, cyclic redundancy checking, and checksum calculation). Such components do not require software programmability and exhibit only a few hardware configuration options.

Furthermore, many NPs incorporate hardware microengines having a behavior resembling that of a simple RISC microprocessor. Such components provide specialized operations for network processing (for example,

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manipulation of bit or byte fields, and network protocol processing) and extensive features for high-level software programmability. It is critical for these components to effectively support many network services, including the provision of an acceptable quality of service. Thus, NPs support the execution of network-specific functions at very high speeds, while remaining flexible because of their programmability. A network end-to-end path involves several such active nodes, each able to process high-bandwidth data, ranging from a few megabits (at the edge network) to several gigabits (in the core network).

As mentioned, many consider NPs the most promising approach to providing both processing power and the required flexibility in the design of networking devices. Because NPs contain special networking functions that are already hardwired, they help reduce time to market. Therefore, although the NP market is still in its infancy, it has been growing steadily. Industry analysts expect this trend to continue; major semiconductor manufacturers have already provided solutions and are focusing on more advanced designs.

The goal of this special issue is to present a consolidated insight into the ongoing research, development, and prototyping of NP systems and applications. We selected five high-quality articles that reflect some of the leading-edge research in NPs. These articles deal with novel NP designs and implementations; simulation tools for performance measurements; specialized software development frameworks for NPs; and the development and evaluation of network- and security-oriented applications on NPs.

The article "Synchronous Dataflow Architecture for Network Processors" introduces a synchronous, pipelined architecture for designing programmable NPs. The proposed pipeline consists of packet processing elements for programmable data manipulation and I/O components for providing access to shared resources. The authors present an actual implementation of the proposed architecture in 0.13-µm CMOS and compare it to other network processing devices.

"PRO3: A Hybrid NPU-Architecture" proposes a novel, programmable network processor architecture for packet processing in multigigabit networks. The architecture uses special-purpose hardware modules, programmable and low-complexity hardware cores, and high-performance, general-purpose RISC cores. The authors present details of the implementation, provide performance measurements, and compare the efficiency of the proposed NP with that of several existing similar devices.

In "NePSim: A Network Processor Simulator with Power Evaluation Framework," the authors present a cycle-accurate simulation tool for analyzing the performance and power dissipation characteristics of NP designs. NePSim is useful in studying the trade-offs between performance and power dissipation in various NP architectures. The article includes experimental data pertaining to four widespread networking applications.

The authors of "NP-Click: A Productive Software Development Approach for Network Processors" deal with the issue of software development for NPs. They present a software development framework tailored to the specialized requirements of NPs and compare it with existing programming approaches, evaluating the achieved performance.

In "Optimization and Benchmark of Cryptographic Algorithms on Network Processors," the authors concentrate on the application of NPs in cryptography. This article analyzes and compares the design of some of the most widely used cryptographic algorithms on an Intel IXP2800. The authors present several optimization directions that can improve the implementation's overall performance.

We believe this special issue supports the claim of the networking community that NPs will probably become the silicon core of network devices that require a high degree of flexibility. As such, NPs will support the evolution of network services that offer extraordinary performance with high packet rates. We hope you will gain valuable information from this issue.

Acknowledgments

For this issue, we received 22 submissions, all of which had at least three reviewers. From that pool, we accepted five, resulting in an acceptance rate of just above 27 percent. Due to a lack of space, we rejected several interesting manuscripts. We thank all the authors for their

manuscripts and the reviewers for their hard work in providing in-depth comments. We also thank *IEEE Micro* Editor-in-Chief Pradip Bose for his constructive advice and support.

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