Design of a Low-Noise Amplifier (RF LNA) for a 5G NR (New Radio) Base Station using GaN and FDSOI Technology

Σχεδίαση Ενισχυτή Χαμηλού Θορύβου *(RF LNA)* για Σταθμό Βάσης *5G NR (New Radio)* με Τεχνολογία *GaN* και *FDSOI*

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Abstract

In the modern era, in order to meet the ever-increasing demand for higher data transmission rates, low latency, enhanced reliability, and massive connectivity, 5G is called upon to provide a foundational technology for future innovations such as autonomous vehicles, industrial automation, and smart cities. Under these conditions, the advanced design of high-performance RF components becomes essential. One of the most important components in a 5G base station RF receiver is the Low Noise Amplifier (LNA). The LNA is designed to amplify weak signals received by the antenna with minimal noise contribution. It must ensure a low noise figure, high gain, good linearity, wide bandwidth, and energy efficiency. Over the past two decades, Gallium Nitride High Electron Mobility Transistors (GaN HEMTs) have been at the forefront of technological advancement, demonstrating significant improvements and playing a crucial role in silicon substrate applications for radio frequency power. This thesis focuses on the design and analysis of an RF Low Noise Amplifier for a 5G NR (New Radio) base station receiver, utilizing GaN technology. The design is based on a Single Stage Common Source LNA with Inductive Degeneration, operating at a 5G frequency band. The main design tool used was the AWR software. The results are notable, achieving a Noise Figure (NF) of 0.65 dB and a Gain of 15.1 dB, powered by a 10V supply and a 0.1V bias voltage. Additionally, an equivalent implementation was carried out using Cadence software for comparative analysis and a deeper understanding of the circuit's behavior. In this case, a 22 nm FDSOI technology was employed, and the achieved performance results include a noise figure (NF) of 0.9 dB, a gain of 21.5 dB, and a linearity figure of –3.27 dBm. These results reflect the effectiveness of the design techniques that were implemented.

Περίληψη

Στη σύγχρονη εποχή, με σκοπό την κάλυψη της συνεχώς αυξανόμενης ζήτησης για υψηλότερους ρυθμούς μετάδοσης δεδομένων, τη χαμηλή καθυστέρηση, την αυξημένη αξιοπιστία και τη μαζική συνδεσιμότητα το $5G$ καλείται να προσφέρει μία θεμελιώδη τεχνολογία για μελλοντικές καινοτομίες όπως αυτόνομα οχήματα, βιομηχανικός αυτοματισμός και «έξυπνες» πόλεις. Υπό αυτές τις συνθήκες, καθίσταται απαραίτητη η προηγμένη σχεδίαση RF στοιχείων με υψηλή απόδοση. Ένα από τα πιο σημαντικά στοιχεία ενός RF δέκτη σε σταθμό βάσης $5G$ είναι ο Ενισχυτής Χαμηλού Θορύβου- **LNA(Low Noise Amplifier)**. Ο LNA έχει σχεδιαστεί ώστε να ενισχύει ασθενή σήματα που λαμβάνει από την κεραία με την ελάχιστη δυνατή προσθήκη θορύβου. Θα πρέπει να εξασφαλίζει χαμηλό δείκτη θορύβου, υψηλό κέρδος, καλή γραμμικότητα, ευρεία ζώνη συχνοτήτων και ενεργειακή απόδοση. Τις τελευταίες δύο δεκαετίες,τα Gallium Nitride High Electron Mobility Transistors βρίσκονται στην αιχμή της τεχνολογικής ανάπτυξης, επιδεικνύοντας σημαντικές προόδους και τον κρίσιμο ρόλο τους σε εφαρμογές υποστρώματος πυριτίου που απαιτούν υψηλή ισχύ στο πεδίο των ραδιοσυχνοτήτων όπως ο σταθμός βάσης. Η παρούσα εργασία επικεντρώνεται στον σχεδιασμό και την ανάλυση ενός Ενισχυτή Χαμηλού Θορύβου RF για δέκτη σταθμού βάσης $5G$ NR (New Radio), αξιοποιώντας την τεχνολογία GaN. Η σχεδίαση έχει ως βάση ένα Single Stage Common Source LNA, με Inductive Degeneration σε συχνότητα λειτουργίας $5G$. Βασικό εργαλείο της, αποτέλεσε το λογισμικό AWR. Τα αποτελέσματα της εργασίας είναι αρκετά ενθαρρυντικά καθώς πετυχαίνει NF 0.65 dB, Gain 15.1 dB, από μία τροφοδοσία 20 Volt και μία τάση πόλωσης 0.1 Volt. Παράλληλα, έγινε αντίστοιχη υλοποίηση στο Cadence για συγκριτική μελέτη και καλύτερη κατανόηση του κυκλώματος. Σε αυτή τη περίπτωση χρησιμοποιήθηκε τεχνολογία 22 nm FDSOI και τα αποτελέσματα που πετυχαίνει αντιστοιχούν σε NF 0.9 dB, Gain 21.5 dB και γραμμικότητα -3.27 dBm, αντανακλώντας την αποτελεσματικότητα των σχεδιαστικών τεχνικών που υλοποιήθηκαν.

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I would also like to thank the company ArgoSemi for providing the workspace where the majority of the work was carried out, as well as for granting access to the design software and offering continuous support throughout the process. I am especially grateful to Mr. Konstantinos Vrysas for providing the specifications of such a demanding circuit, as well as for his valuable advice and constant guidance.

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I extend my warm thanks to my friends Anastasia and Eugenia, and to my partner Manolis, for their unwavering support throughout my studies. Their companionship, encouragement, and understanding significantly contributed to my mental well-being and the smooth completion of this project.

Finally, I wish to express my deepest gratitude to my parents, Paraskevi and Konstantinos, as well as to my siblings Athina and Giorgos, who stood by me with unconditional love, understanding, and trust at every step of this journey. Their encouragement and belief in my abilities have been invaluable throughout my academic years. I dedicate this thesis to them as a small token of appreciation for all they have given me.

Abbreviations

Abbreviation	Meaning
2DEG	Two-Dimensional Electron Gas
AlGaN	Aluminum Gallium Nitride
CMOS	Complementary Metal-Oxide-Semiconductor
CG	Common Gate
CS	Common Source
FD-SOI	Fully Depleted Silicon-on-Insulator
GaAs	Gallium Arsenide
GaN	Gallium Nitride
GNSS	Global Navigation Satellite System
HEMT	High-Electron-Mobility Transistor
IP3	Third-Order Intercept Point
LNA	Low Noise Amplifier
mmWave	Millimeter Wave
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
mMTC	Massive Machine-Type Communications
NF	Noise Figure
NFET	N(P)-Channel Field Effect Transistor
NR	New Radio
P1dB	1 dB Compression Point
PA	Power Amplifier
PD-SOI	Partially Depleted Silicon-on-Insulator
PSD	Power Spectral Density
RF	Radio Frequency
RMS	Root Mean Square
SiC	Silicon Carbide
SLVT	Super Low V_T
SNR	Signal-to-Noise Ratio
SOI	Silicon-on-Insulator

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Chapter 1

Introduction

1.1 Understanding 5G and LNAs

In recent years, the number of people and devices connected to the internet has increased dramatically. At the same time, the evolution of the Internet of Things (IoT) - the concept that many devices can be interconnected to create a larger network - has enabled a wide range of applications across different domains and organizations. The development of smart homes, smart vehicles, energy management systems, and remote work infrastructure requires a highly reliable and extremely fast internet connection. This growing need for high-speed connectivity is a major driver behind the expansion and establishment of 5G technology.

5G NR (New Radio), standardized by the 3rd Generation Partnership Project (3GPP), defines a new radio access technology that surpasses the capabilities of previous generations, such as LTE, while offering a highly flexible and scalable platform to meet the demands of future applications. It can operate across a broad frequency range - from sub-1 GHz bands, which ensure wide coverage, to millimeter wave (mmWave) frequencies, which enable ultra-high data transmission speeds. One of its key features is scalable numerology, which allows the use of different subcarrier spacings for optimal performance in various deployment scenarios, such as enhanced Mobile Broadband (eMBB), Ultra-Reliable Low Latency Communications (URLLC), and massive Machine-Type Communications (mMTC).

To achieve the high performance promised by 5G NR, the efficient design of the receiver chain is essential. A critical component of this chain is the Low Noise Amplifier (LNA), which is responsible for amplifying the weak received signal while introducing minimal additional noise, thereby preserving a high signal-to-noise ratio (SNR). The efficiency of the LNA is particularly important in the mmWave frequency bands, where signals are subject to greater

attenuation due to propagation characteristics.

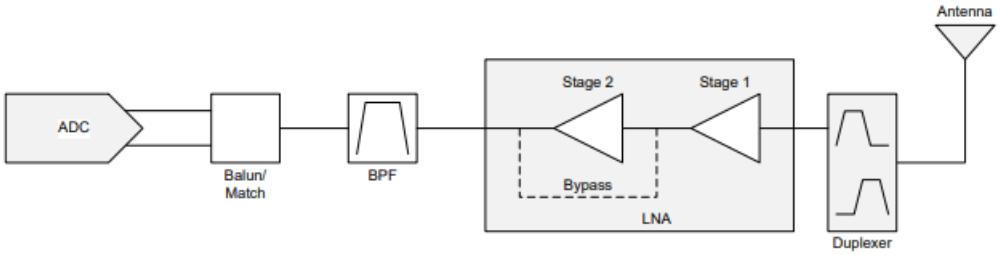


Figure 1.1: RF Sampling Receiver Chain[1]

The design of LNAs for 5G applications must meet stringent requirements, including low noise figure, high gain, good linearity, wide bandwidth, and power efficiency. Additionally, the use of advanced semiconductor technologies such as Gallium Nitride (GaN) offers promising benefits for achieving high performance in LNA design, particularly at high frequencies and under high-power conditions.

This thesis focuses on the design and analysis of an RF Low Noise Amplifier for a 5G NR (New Radio) base station receiver, utilizing GaN technology. The objective is to achieve optimal noise performance and gain while meeting the frequency and power requirements of modern 5G systems.

1.2 Outline

⋆ **Chapter 2: RF Design and LNAs**

Provides a comprehensive overview of RF design principles, with a particular focus on Low Noise Amplifier (LNA) applications and the analysis of various noise types - an essential concept in LNA design theory.

⋆ **Chapter 3: Low Noise Amplifier Design Considerations**

Explores the fundamental design parameters of LNAs and presents key amplifier topologies commonly used in practical implementations.

⋆ **Chapter 4: GaN HEMT Technology**

Discusses Gallium Nitride (GaN) HEMT technology, highlighting its advantages and limitations,

and compares it with alternative technologies such as GaAs pHEMT.

⋆ **Chapter 5: Low Noise Amplifier Design**

Presents a detailed methodology for designing the proposed LNA, including schematic development, simulation results, and a performance comparison with existing designs.

⋆ **Chapter 6: Conclusion**

Summarizes the key findings, provides final remarks, and proposes directions for future research in LNA and RF front-end design.

Chapter 2

RF Design and LNAs

2.1 What exactly is a Low Noise Amplifier

A Low Noise Amplifier (LNA) is a critical component in the front-end of a wireless receiver, serving as the first stage of signal amplification. Its primary objectives are to amplify weak radio frequency (RF) signals captured by the antenna and to minimize the introduction of additional noise, thereby preserving the integrity of the received signal. The LNA is specifically designed to provide sufficient gain while maintaining a low noise figure, ensuring that the signal remains discernible and usable for subsequent processing stages. Due to its position at the initial stage of the receiver chain, the performance of the LNA significantly influences the overall sensitivity and noise performance of the entire system.

2.2 Applications of LNAs

The LNAs ability to amplify low signals while adding minimal noise makes them indispensable in numerous high-frequency applications. Some of the most common and critical areas where LNAs are employed include:

2.2.1 Satellite Communication

The role of Low Noise Amplifiers (LNAs) is particularly critical in satellite ground stations and onboard satellite transceivers, due to the extremely weak signals received from space. They are commonly employed in low-noise block downconverters (LNBs) to amplify and downconvert

signals for satellite television and data reception. LNAs are also essential components in GPS and other Global Navigation Satellite System (GNSS) receivers, as they are responsible for amplifying the signals transmitted by satellites in Earth's orbit. Both the signal integrity and the reliability of positioning accuracy heavily depend on the noise performance of the LNA.

2.2.2 Radar Systems

Radar systems (Radio Detection and Ranging) operate by transmitting electromagnetic waves and analyzing the reflected signals to detect and localize objects. Often, the reflected signals are extremely weak, making the role of the Low Noise Amplifier (LNA) critical in the radar receiver front-end. LNAs are essential in enhancing the detectability of these signals without significantly degrading their quality. Some of the radar systems that heavily rely on LNAs include automotive radar, military radar, weather radar, as well as aviation and air traffic control radar systems.

2.2.3 Wireless Communication Systems

In modern wireless networks such as 4G LTE, 5G New Radio (NR), Wi-Fi, and Bluetooth, the operating frequencies are continuously increasing, and signal environments present significant challenges due to interference, noise, and high-loss propagation paths—especially in dense urban areas. As a result, LNAs must deliver low noise figure, high gain, and excellent linearity with minimal power consumption. They are widely used in mobile devices, base stations, Wi-Fi routers, 5G mmWave systems, and IoT applications to ensure reliable and efficient signal reception.

2.3 Noise in RF Systems

One of the most critical challenges in communication systems is noise. Noise is defined as any signal other than the desired one. An unavoidable source of electrical noise is the random thermal motion of electrons in wires, resistors, and consequently in active circuits. If noise did

not exist in nature, RF receivers would be able to detect arbitrarily small signals from arbitrarily long distances. However, detecting extremely weak signals is not realistic, as the presence of noise sets a lower limit on the minimum detectable signal. The main sources that contribute to noise in a system are presented below:

2.3.1 Thermal Noise

Thermal noise originates from the random motion of charge carriers within an electrical conductor caused by thermal energy. This phenomenon was first observed by Johnson (1928) and was mathematically formulated by Nyquist thus, thermal noise is also known as Johnson-Nyquist noise. It is one of the most common sources of noise in electronic circuits and plays a critical role in the performance of communication systems, electronic devices, and measurement systems.

Unlike other forms of noise, thermal noise is always present in a system at any temperature and is independent of the current flowing through the circuit. It is classified as white noise, meaning that its power spectral density (PSD) is flat across a wide range of frequencies, leading to a uniform power distribution over frequency. In the time domain, the amplitude of thermal noise follows a Gaussian probability distribution, meaning most values are centered around the mean, with fewer values occurring as one moves further from the mean.

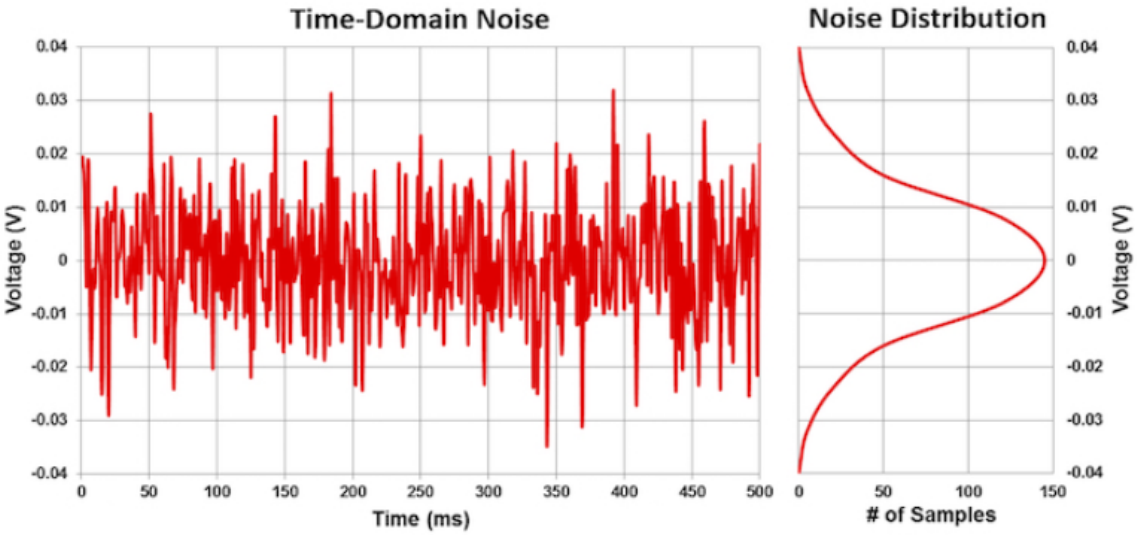


Figure 2.1: Thermal Noise at the left graph and Gaussian Distribution curve at the right graph.[2]

The main parameters that affect thermal noise are:

- **Temperature (T)**: At higher temperatures, the electrons in a material possess more kinetic energy, resulting in increased random motion and consequently larger fluctuations in current and voltage. Conversely, at lower temperatures, electron motion is reduced, leading to lower thermal noise levels.

- **Resistance (R)**: Any resistive material generates noise due to the thermal agitation of electrons within the material. The thermal noise voltage is directly proportional to the resistance value, meaning that higher resistance produces more thermal noise.

- **Bandwidth (B)**: Bandwidth refers to the range of frequencies over which the system operates or processes signals. In the context of thermal noise, a wider bandwidth allows more noise power to pass through the system, while a narrower bandwidth reduces the noise.

Power Spectral Density(PSD)

The thermal noise voltage across a resistor is described by the power spectral density (PSD).

$$S_v(f) = 4k_BTR \tag{2.1}$$

where, $S_v(f)$ is the power spectral density of the noise voltage, k_B is the Boltzmann's constant, T is the absolute temperature in Kelvin (K) and R is the resistance.

Total Noise Power

In order to find the total noise power P_n over a certain bandwidth B, the spectral density can be integrated over the bandwidth. The noise power is given by:

$$P_n = 4k_BTRB \tag{2.2}$$

where, B is the bandwidth of the measurement in Hertz (Hz).

Root Mean Square (RMS) Voltage

The noise power can also be expressed in terms of voltage by taking the square root of the power over bandwidth.

$$V_{\text{rms}} = \sqrt{4k_BTRB} \tag{2.3}$$

2.3.2 Shot Noise

Shot noise, or Poisson noise, is a type of noise that arises due to the discrete nature of electric charge or other particles. The concept of shot noise became widely known through the work of Walter Schottky (1918), who studied current fluctuations in vacuum tubes. It is of particular importance in situations where particle detection is performed in a quantized manner, such as in electronics or photonics. Shot noise follows a Poisson statistical distribution, reflecting the random and independent nature of particle arrivals. This implies that the variance (σ^2) in the number of particles arriving in a given time interval is equal to the mean (μ).

Furthermore, shot noise exhibits a flat or "white" power spectral density, which indicates that its intensity remains constant across all frequencies up to a certain limit. The flat spectrum is a direct consequence of the random and uncorrelated nature of particle arrivals. In contrast to thermal noise, which is temperature-dependent, shot noise is independent of both temperature and frequency.

Mathematically, the Power Spectral Density (PSD) for shot noise is given by:

$$S_I = 2e|I| \tag{2.4}$$

where S_I represents the power spectral density, e is the elementary charge (1.6×10^{-19} C), and I denotes the average current.

2.3.3 Flicker Noise

Flicker noise, also known as *1/f noise* or *pink noise*, decreases with increasing frequency. Like many other noise sources, it is difficult to predict accurately. It plays an important role in many electronic systems, especially in oscillators used as radio frequency sources. In contrast to shot noise, the power spectral density of flicker noise increases as the frequency decreases. For this reason, it is also referred to as low-frequency noise. The bandwidth of flicker noise typically ranges from approximately 10 MHz down to 10 Hz.

This phenomenon is mainly observed in semiconductors used in instrumentation amplifiers

for recording electrical signals. It is generated by defects at the interface between the silicon dioxide gate and the silicon substrate. Traps in the silicon crystal - associated with crystal imperfections - capture and release charge carriers randomly, producing flicker noise. Generally, this noise dominates system performance at low frequencies, even in well-designed circuits, and is inversely proportional to frequency.

This noise can be expressed as:

$$S(f) = \frac{K}{f^{\alpha}} \tag{2.5}$$

Where, $S(f)$ is the power spectral density at frequency f, K is a constant depending on the physical characteristics of the system, and α is a dimensionless exponent typically close to 1, usually in the range $0.8 \leq \alpha \leq 1.2$.

Corner Frequency

The "Corner frequency" is defined as the frequency where the flicker and thermal noise equalize.

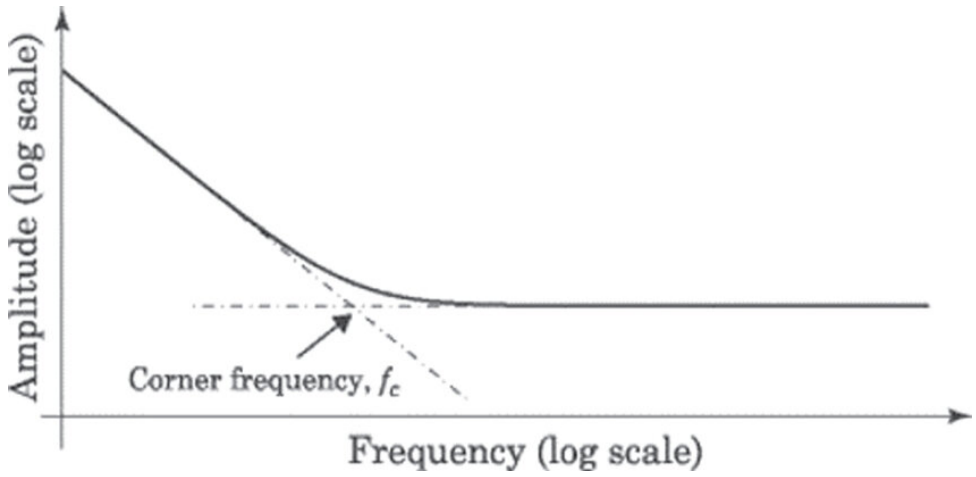


Figure 2.2: Corner Frequency.[3]

Noise significantly affects signal quality and is a major concern in communication system design. Its minimization is essential for ensuring reliable performance. Two primary techniques are used: **passive noise control**, which employs non-powered insulating materials, and **active noise control**, which uses powered components to reduce or cancel noise, often by increasing signal gain.

Noise degrades the signal-to-noise ratio (SNR), limiting the system's ability to accurately transmit and receive data. Maintaining a high SNR is crucial, especially in modern communication

systems. Thus, achieving a careful balance between signal amplification and noise suppression is key to optimizing overall system performance.

Chapter 3

Key Factors in Low Noise Amplifier Design

3.1 Target Specifications

The design of a Low Noise Amplifier (LNA) requires careful planning and evaluation of certain critical parameters that directly affect the LNA's performance in a communication system. Based on these parameters, the ability of the LNA to effectively amplify weak signals while minimizing noise is determined. Therefore, the design of LNAs is governed by the following parameters:

3.1.1 Noise Performance

As previously mentioned, the amplifier will amplify both the input signal and the noise present at the input. At the same time, intrinsic noise sources within the transistor will propagate toward the output signal, introducing additional noise at the output. The *Noise Figure (NF)* of an LNA is a critical parameter that affects the overall noise of a receiver system. Minimizing the noise introduced by the amplifier is essential in achieving a high signal power with a favorable signal-to-noise ratio (SNR). The mathematical expressions describing the *Noise Factor (F)* and the *signal-to-noise ratio (SNR)* are presented below.

$$F = \frac{\text{SNR}_{\text{in}}}{\text{SNR}_{\text{out}}} \quad (\text{dB}) \tag{3.1}$$

$$\text{SNR} = \frac{P_{\text{signal}}}{P_{\text{noise}}} \quad (\text{dB}) \tag{3.2}$$

If the Noise Factor is expressed in decibels it is called the *Noise Figure(NF)*.

$$NF_{\text{dB}} = 10 \cdot \log_{10}(F) \tag{3.3}$$

In an ideal scenario, in a noise-free LNA, the noise factor would be equal to unity. Minimizing noise imposes constraints on both the circuit topology choices and the number of amplifying stages.

In multi-stage amplifier systems, such as RF receivers, the overall noise performance depends on the noise and gain characteristics of each stage. The **Friis formula** is used to calculate the total *Noise Factor* F_{total} of a cascaded system:

$$F_{\text{total}} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots + \frac{F_n - 1}{G_1 G_2 \cdots G_{n-1}} \tag{3.4}$$

Where:

- F_i is the noise factor of the i-th stage (in linear scale),
- G_i is the power gain of the i-th stage (also in linear scale),
- F_1 and G_1 refer to the first stage, which usually has the most significant impact on the total noise.

$$NF = 10 \log(F) = 10 \left(\frac{\text{SNR}_{\text{in}}}{\text{SNR}_{\text{out}}} \right) \quad \text{(dB)} \tag{3.5}$$

3.1.2 Gain

Gain in an amplifier is a measure of its ability to increase the power or amplitude of a signal. It is usually defined as the average ratio of the output signal of a system to the input signal of the same system. The LNA is the first block in a receiver; therefore, high gain and low noise figure are essential in its design. In amplifiers and generally in RF systems, there are different types

of gain, each describing a different aspect of signal amplification. Below are the most common types of gain encountered — especially in Low Noise Amplifiers (LNAs):

- **Power Gain (G_P)** represents the ratio of power delivered to the load to the power absorbed at the input:

$$G_P = |S_{21}|^2 \tag{3.6}$$

  This assumes conjugate matching at the output and that the input is matched as well.

- **Voltage Gain (A_V)** is given by:

$$A_V = \left| \frac{S_{21}}{(1 - S_{11}\Gamma_S)(1 - S_{22}\Gamma_L)} \right| \tag{3.7}$$

  But this is not a standard representation — voltage gain is typically calculated through circuit analysis rather than S-parameters directly. For matched networks, it's often approximated by

$$A_V \approx |S_{21}| \tag{3.8}$$

- **Transducer Gain (G_T)** signifies the ratio of power delivered to the load to the power available from the source:

$$G_T = \frac{1 - |\Gamma_S|^2}{|1 - S_{11}\Gamma_S|^2} \cdot |S_{21}|^2 \cdot \frac{1 - |\Gamma_L|^2}{|1 - S_{22}\Gamma_L|^2} \tag{3.9}$$

- **Available Power Gain (G_A)** indicates the ratio of available output power to available power from the source:

$$G_A = \frac{|S_{21}|^2(1 - |\Gamma_S|^2)}{|1 - S_{11}\Gamma_S|^2(1 - |S_{22}|^2)} \tag{3.10}$$

  This is the gain when the load is conjugately matched to the output, and the source may not be matched.

3.1.3 Centre Frequency and Bandwidth

The operation of a Low Noise Amplifier (LNA) is based on the amplification of an input signal that resides within a specific frequency range. Therefore, its design must be optimized around a central frequency f_0 and a corresponding bandwidth Δf. The frequency response of the LNA, typically characterized by its transfer function, determines the range of frequencies over which the amplifier provides sufficient gain. The bandwidth Δf is defined as the frequency range between the two -3 dB points on either side of the central frequency f_0, where the power gain falls to half of its peak value. This parameter is critical in ensuring that the LNA effectively amplifies all relevant signal components without significant distortion or attenuation across the desired frequency spectrum.

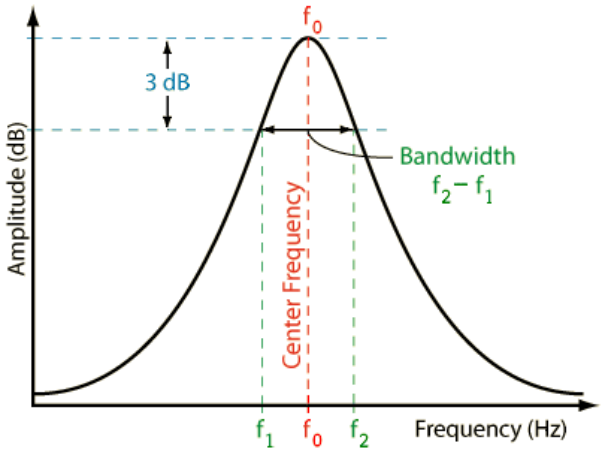


Figure 3.1: Centre frequency and Bandwidth.[4]

Depending on the application, LNAs may be designed for either narrowband or wideband operation, the choice directly impacts the amplifier's architecture, stability, and noise performance. A narrowband LNA operates over a relatively small frequency range centered around f_0, providing high gain and optimized performance for a specific frequency channel. On the other hand, wideband LNAs are designed to cover a broad frequency range.

3.1.4 Input and Output Impedance Matching

Impedance matching is a critical consideration in RF design, as it not only ensures maximum power transfer but also allows for achieving the highest possible gain. Input impedance matching,

in particular, is essential for maximizing the power transferred from the source to the amplifier, thereby improving the overall performance of the system.

The filter placed between the antenna and the LNA is typically designed with a standard termination impedance of 50 Ω. If the impedance seen at the input of the LNA — through the filter — deviates from this 50 Ω standard, it can lead to increased signal loss and reflection. Therefore, to achieve effective input impedance matching, the LNA must be designed to present an input impedance of 50 Ω, which corresponds to a reflection coefficient $\Gamma = 0$.

It is important to note that in this context, power matching is equivalent to impedance matching. Proper matching at both the input and output is vital to minimize signal degradation and ensure efficient signal amplification throughout the RF chain.

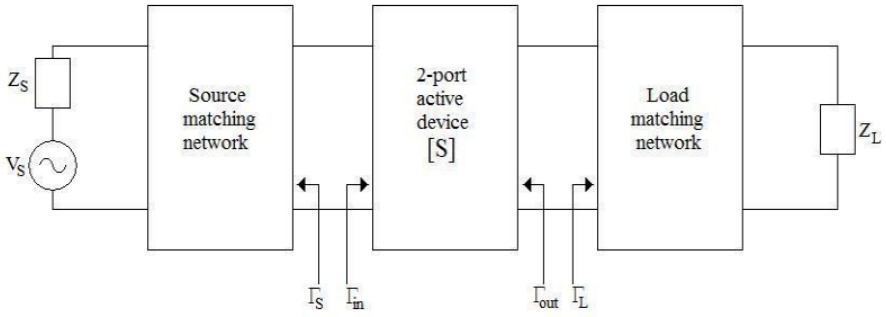


Figure 3.2: Conjugate matching in a two - port network.[5]

For a two-port network, the problem of impedance matching can become even more complex.

The input reflection coefficient Γ_{in} is given by:

$$\Gamma_{in} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \tag{3.11}$$

The output reflection coefficient Γ_{out} is given by:

$$\Gamma_{out} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \tag{3.12}$$

Where:

- S_{ij} are the S-parameters of the two-port network.
- Γ_S is the source reflection coefficient.
- Γ_L is the load reflection coefficient.

In the context of a 2-port network, conjugate matching refers to the condition where the input and output impedances of the amplifier are the complex conjugates of the source and load impedances, respectively.

This condition is satisfied when:

$$\Gamma_{\text{in}} = \Gamma_S^* \quad \text{and} \quad \Gamma_{\text{out}} = \Gamma_L^* \tag{3.13}$$

Achieving output matching plays a significant role in the stability of the amplifier, ensuring the effective delivery of the amplified signal to subsequent stages. Any deviation from conjugate matching results in increased signal reflections and degrades the overall performance of the amplifier.

3.1.5 Linearity

Another critical parameter that must be considered in LNA design is linearity. Linear operation is essential, particularly when a weak input signal is accompanied by a nearby strong interfering signal, as it can lead to undesirable distortion. The two primary measures of linearity are the Third-Order Intercept Point (IP3) and the 1-dB Compression Point (P1dB).

The Third-Order Intercept Point (IP3) indicates the power level at which the third-order intermodulation products become equal in power to the fundamental output signal. The input and output powers corresponding to this point are referred to as IIP3 and OIP3, respectively.

The P1dB Compression point represents the input power level at which the output power drops by 1 dB from the ideal linear gain due to nonlinearity. Knowing either IP3 or P1dB allows the estimation of the other, as they are related by the following expression:

$$\text{IP3} \approx \text{P}_{1\text{dB}} + 10\,\text{dB} \tag{3.14}$$

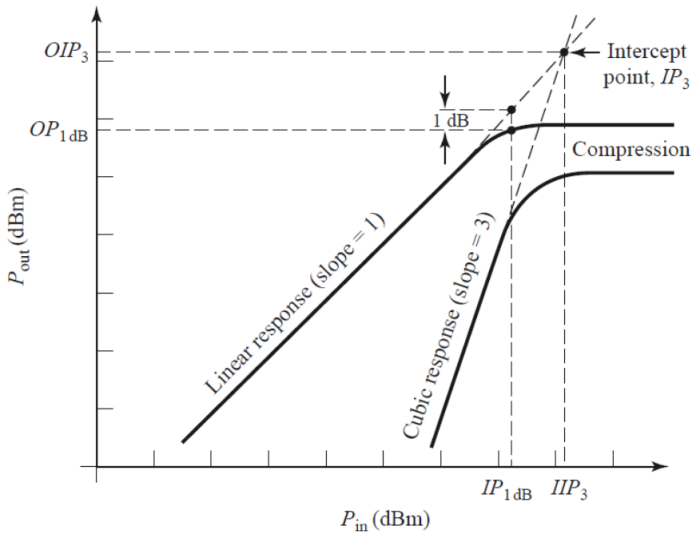


Figure 3.3: Third order intercept point and P1dB Compression point.[6]

The ratio between the maximum input signal power (typically at the 1-dB compression point) and the minimum detectable signal (typically defined by the noise floor or sensitivity of the system), is defined as the dynamic range(DR).

$$\text{Dynamic Range (dB)} = P_{1\text{dB}} - \text{Noise Floor} \tag{3.15}$$

A wider dynamic range allows a system to detect weak signals while still handling strong signals without distortion — crucial in communication receivers, radar, and other RF applications.

3.1.6 Stability

Assuming that the LNA is required to operate within a desired frequency band, any tendency to oscillate at other frequencies may lead to highly nonlinear behavior and significantly compressed gain. Therefore, the LNA must remain stable across all source impedance and frequency variations. An LNA can be either *unconditionally stable* or *potentially unstable*.

In a two-port network, oscillations may occur if certain source and load terminations cause the input or output impedance to exhibit a negative real part. The condition for unconditional

stability, expressed in terms of S-parameters, is given by the following inequalities:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1 \tag{3.16}$$

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1 \tag{3.17}$$

If $K > 1$ and $|\Delta| < 1$, the circuit is unconditionally stable, indicating that it will not oscillate for any combination of source or load impedance. Achieving an unconditionally stable LNA is a fundamental design requirement for maintaining signal integrity and overall system reliability.

3.2 Low Noise Amplifier Topologies

The characteristics of an LNA are determined not only by the active device and the matching network, but also by their topology. This section presents the fundamental aspects of LNA topologies, including the classical configurations such as common gate, common source, and cascode stages, analyzing their advantages, disadvantages, and associated design challenges.

3.2.1 Common - Source LNA with Inductive Source Degeneration

In an LNA, one of the main contributors to an increased noise figure is the use of resistive components. To overcome this limitation, inductive source degeneration is employed as a substitute for resistive source degeneration. This topology is highly effective in achieving a low noise figure and reduced power consumption, making it essential for many industrial applications, though primarily suited for narrowband operations.

The Common-Source (CS) configuration is a fundamental amplifier topology where the input signal is applied to the gate of a MOSFET, the output is taken from the drain, and the source terminal is common (either grounded or connected via a passive component). The term

”degeneration” refers to the insertion of an element — in this case, an inductor L_s — in series with the source of the transistor.

Inductive degeneration introduces negative feedback, which enhances circuit stability, provides input impedance matching, and contributes to noise reduction by lowering the noise resistance of the amplifier.

The input impedance of this topology is approximated by the following expression:

$$Z_{\text{in}} \approx j\omega L_s + \frac{1}{j\omega C_{gs}} + g_m L_s \tag{3.18}$$

With proper selection of the source inductor L_s, input impedance matching to 50 Ω can be achieved effectively.

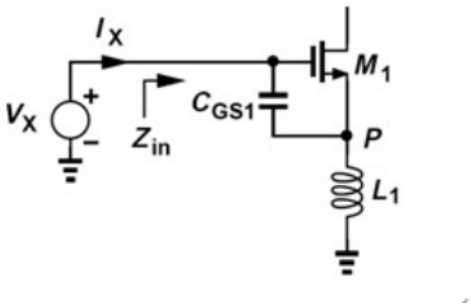


Figure 3.4: Common - Source stage with inductive degeneration.[7]

The feedback introduced through the gate-drain capacitance C_{gd} can be utilized to generate the required real component of the input impedance. However, this feedback may also induce a negative resistance at lower frequencies, potentially affecting circuit stability. In the expression for input impedance (3.18) the third term $g_m L_s$ contributes a real component that can be designed to match the standard $50\ \Omega$ input impedance. In practical implementations, the degeneration inductor L_s is often realized using the bond wire inductance, as this element is inherently present due to the packaging of the integrated circuit. Incorporating this unavoidable parasitic inductance into the design not only facilitates impedance matching but also helps reduce additional layout complexity.

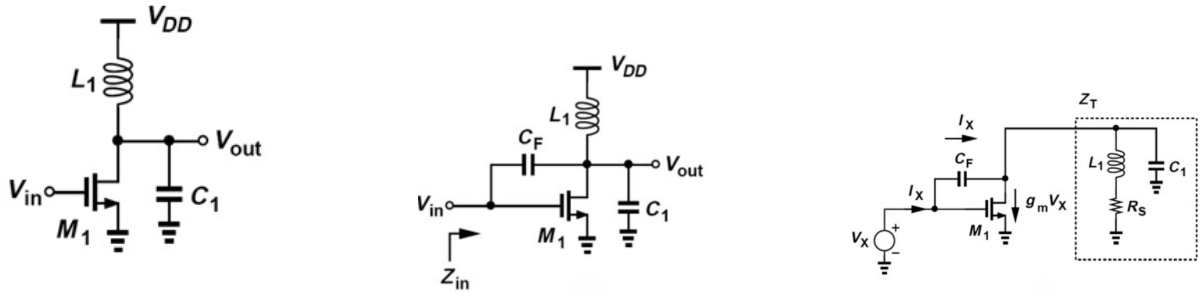
3.2.2 Common - Source LNA with Inductive Load

This topology represents one of the most widespread and fundamental configurations for implementing an LNA in RF applications. The input signal is applied to the **gate** of the transistor, the **source** is typically grounded or includes a degeneration element, and the **output** is taken from the **drain**, where an inductive load is connected instead of a simple resistive one.

In general, the trade-off between voltage gain and supply voltage in a Common-Source (CS) stage with a resistive load makes it less attractive, particularly as the supply voltage continues to scale down with modern technologies. For instance, at low frequencies, the voltage gain is given by:

$$|A_v| = g_m R_D = \frac{2I_D}{V_{GS} - V_{TH}} \cdot \frac{V_{RD}}{I_D} = \frac{2V_{RD}}{V_{GS} - V_{TH}} \tag{3.19}$$

To circumvent this limitation and to enable operation at higher frequencies, the CS stage can incorporate an inductive load. This configuration allows operation with very low supply voltages, since the inductor requires a smaller DC voltage drop compared to a resistor. Additionally, the LC tank circuit at the drain can be tuned to the desired center frequency, enabling narrowband operation of the LNA. The use of an inductive load allows for achieving high gain while also improving noise performance at the resonance frequency.



(a) (b) (c)

Figure 3.5: (a) Common-Source stage with inductive load, (b) Input Impedance including C_F, (c) Equivalent Circuit.[8]

The circuit in Figure 3.5(b) is a more complete model due to the inclusion of C_F, which represents the gate-drain overlap capacitance, and aims at the computation of the input impedance Z_{in}.

Accordingly, in the modified circuit of Figure 3.5(c), circuit analysis can be performed by taking into account the series resistance R_s, leading to the following expressions:

$$Z_T = \frac{L_1 s + R_s}{L_1 C_1 s^2 + R_s C_1 s + 1} \tag{3.20}$$

The addition of the voltage drop across C_F to the tank voltage results in:

$$V_X = \frac{I_X}{C_F s} + (I_X - g_m V_X) Z_T \tag{3.21}$$

where $I_X - g_m V_X$ is the current flowing through the output network.

The presence of capacitance C_F introduces feedback from the output to the input, which can lead to negative input resistance and, consequently, to amplifier instability. To address this issue, inductive neutralization is employed, where an inductor L_F is placed in series with the drain or near the gate terminal. This element forms a parallel resonance with C_F at the desired operating frequency, effectively neutralizing the feedback and enhancing stability.

3.2.3 Common - Gate LNA with Inductive Load

The low input impedance exhibited by this topology makes it highly attractive for LNA design. The Common-Gate (CG) topology is capable of offering low noise at high frequencies, and for this reason, it is widely used in broadband RF applications. Special attention must be given to the parasitic input capacitances, as they are the main limiting factor for the amplifier's performance at high frequencies.

However, the CG topology with an inductive load is primarily considered, as illustrated in Figure 3.6(a). The inductor L_1 resonates with the total capacitance at the output node, while the resistor R_1 models the losses of the inductor L_1.

If channel-length modulation and body effect are neglected, then the input resistance of the CG stage is given by:

$$R_{\text{in}} = \frac{1}{g_m}$$

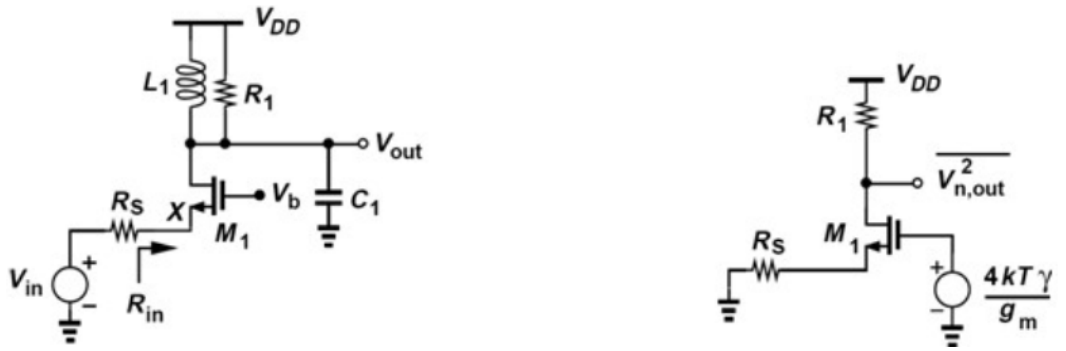
The voltage gain from node X to the output node at the resonance frequency, as shown in Figure 3.6(a), is:

$$\frac{V_{\text{out}}}{V_X} = g_m R_1 = \frac{R_1}{R_S}$$

Finally, the noise figure (NF) of the circuit can be estimated by modeling the thermal noise as a voltage source in series with the gate input, as shown in Figure 3.6(b). The expression for the noise figure (NF) of the circuit is given by:

$$NF = 1 + \gamma + \frac{4R_S}{R_1}$$

It is therefore evident that increasing g_m leads to a lower noise figure but at the same time reduces the input resistance, thus negatively affecting the input matching.



(a) (b)

Figure 3.6: (a) Common-Gate stage with inductive load, (b) Noise contribution of M1.[8]

3.2.4 Comparison Between CS and CG Cascode LNA Topologies

Taking into account the analysis of the Common-Gate and Common-Source topologies presented earlier, the choice between the two depends on the design requirements — whether the goal is precise input matching or the minimization of the noise figure.

The Common-Source topology can achieve a low Noise Figure (NF < 2 dB) and provides a high voltage gain. However, it exhibits significant sensitivity to packaging parasitic capacitances. On the other hand, the Common-Gate topology offers natural input matching and wideband behavior, at the cost of a higher noise figure (NF ~ 4 dB) and reduced amplifier gain.

Chapter 4

GaN - HEMT Design Technology

4.1 Introduction to Gallium Nitride High Electron Mobility Transistors

A fundamental component in LNAs used in RF (front-end) receivers is the **GaAs pHEMT** technology. However, the need to meet increasingly demanding requirements—such as high linearity, low noise, and enhanced robustness—drives the development of new semiconductor technologies and novel LNA design techniques.

At this point, **GaN HEMT (Gallium Nitride High Electron Mobility Transistor)** technology emerges as a highly attractive wide dynamic range solution for the implementation of microwave front-end components. GaN HEMT devices are based on an **AlGaN/GaN heterojunction**, which forms a *barrier-free two-dimensional electron gas (2DEG) channel*. Unlike GaAs pHEMT technology, GaN HEMTs offer a wide bandgap, high breakdown voltage, high electron mobility, and excellent thermal conductivity. These characteristics translate into significant improvements in output power and amplifier linearity.

In modern applications, GaN HEMTs are deployed across a wide range of advanced technological domains. They are used in the development of both power amplifiers (PAs) and low-noise amplifiers (LNAs) for base station (RBS) front-ends in *4G, 5G, and 6G wireless communication networks*. They also serve as key components in *active electronically scanned array (AESA) radar systems*, used in both military and civilian applications, such as *autonomous vehicles*, *unmanned aerial vehicles (UAVs)*, and *air traffic control systems*. Furthermore, GaN HEMTs are critical in *satellite communications*, *space systems*, *millimeter-wave sensors*, and *terahertz (THz) technologies* for imaging and spectroscopy, owing to their thermal stability and

high-voltage efficiency.

Finally, their ability to handle high power levels without the need for additional protection circuitry makes GaN HEMTs particularly attractive for robust RF front-end systems, contributing to reduced system complexity and overall cost.

4.2 Fundamental Theoretical Analysis of Gallium Nitride HEMT Devices

4.2.1 Structure of GaN HEMT

A GaN HEMT is a type of field-effect transistor that utilizes the unique properties of a heterojunction formed between Aluminum Gallium Nitride (AlGaN) and Gallium Nitride (GaN) materials. A basic AlGaN/GaN HEMT design is depicted below.

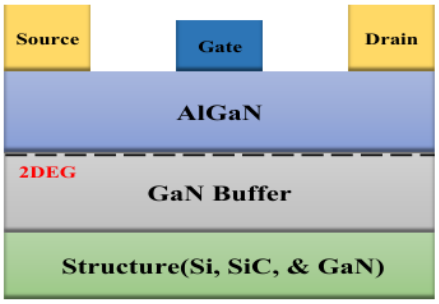


Figure 4.1: AlGaN/GaN HEMT layout and 2DEG generated are shown by the dashed line.[9]

GaN HEMTs operate in two modes: depletion mode and enhancement mode. In Depletion Mode (D-mode), the transistor is normally-on when the gate voltage is zero. This occurs because a two-dimensional electron gas (2DEG) is naturally formed at the AlGaN/GaN interface, functioning as a conductive channel even without any applied gate voltage. To turn the transistor off and stop the current flow, a negative gate voltage must be applied, which reduces or eliminates the 2DEG.

On the other hand, in Enhancement Mode (E-mode), the transistor is normally-off, and the 2DEG is absent at zero gate voltage. The gate is designed to suppress the formation of the

conductive channel under no bias conditions. Applying a positive gate voltage activates the device, allowing the formation of the 2DEG and restoring current conduction. E-mode GaN HEMTs are particularly attractive for power and RF applications as they offer safer operation, high reliability, and compatibility with logic-level control circuits.

What exactly is the 2DEG?

A key feature of HEMT devices is the formation of a two-dimensional electron gas (2DEG), enabled by the combined effect of two types of polarization: piezoelectric polarization (P_{pz}) and spontaneous polarization (P_{sp}), occurring at the AlGaN/GaN heterointerface. This phenomenon creates an intrinsic conductive channel, allowing the device to remain in an on-state without requiring external gate bias. Both GaN and AlGaN exhibit significant spontaneous polarization. When mechanical strain is applied, piezoelectric polarization (P_{pz}) is also generated in the GaN or AlGaN layers.

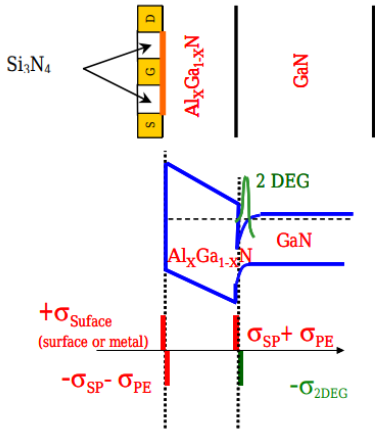


Figure 4.2: Band diagram and origin of 2DEG in AlGaN/GaN HEMTs. (σ: Charge, SP: Spontaneous Polarization, PE: Piezoelectric Polarization).[10]

This piezoelectric polarization is induced in the thin AlGaN layer due to tensile strain, while the GaN layer, being much thicker, remains nearly relaxed in the AlGaN/GaN heterostructure. Therefore, the 2DEG naturally forms at the interface when a thin, strained AlGaN layer is grown on top of a thicker, relaxed GaN layer. Due to the confinement of high-mobility electrons, this 2DEG exhibits excellent conductivity within the quantum well.

In HEMT structures, the formation of a channel with high mobility and electron density is ideal. The substrates used are typically SiC, silicon, sapphire, or GaN, and a buffer layer is introduced to relieve strain resulting from lattice mismatch with the foreign substrate.

The GaN HEMT device, with the 2DEG established at the AlGaN/GaN interface, modulates the gate-source voltage (V_{GS}) to generate a vertical electric field. This field either depletes or enhances the channel, reducing conductivity in the off-state or increasing it in the on-state.

4.2.2 Lateral and Vertical GaN Power Transistors

In ***lateral GaN HEMTs***, the gate, source, and drain are all on top with the gate sitting on the AlGaN layer, and the source and drain electrodes piercing through the AlGaN layer to form an ohmic contact with the underlying 2DEG, which is where current flow occurs. The lateral structure of the GaN HEMT is illustrated in Figure 4.3.

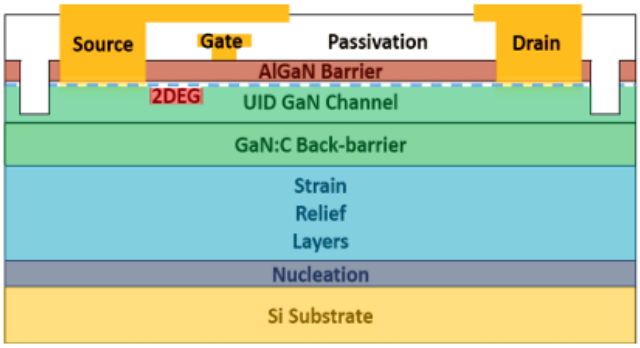


Figure 4.3: A typical lateral AlGaN/GaN HEMT structure.[9]

The AlGaN/GaN structure is characterized by high electron mobility (2000 $cm^2/V{\cdot}s$) and high electron velocity (1.3×10^7 cm/s saturation velocity and 2.5×10^7 cm/s peak velocity). GaN HEMTs exhibit low on-resistance due to their high carrier concentration and increased electron mobility.

D-mode GaN devices are *normally-on*, and current flows between the drain and the source even without applying any potential to the gate. When such devices are used, the switch must be turned off before powering up the converter to avoid a short circuit at startup. For this reason, d-mode GaN HEMTs are not used as stand-alone switches in power conversion applications.

GaN HEMTs used in power converters are required to be *normally-off* devices to ensure safe operation. If the gate driver is disabled or fails and its output is zero, the HEMT must remain turned off. To achieve this, the d-mode GaN structure must be modified. Two common solutions are:

1. **p-GaN Gate**: The insertion of a p-GaN or p-AlGaN layer between the gate and the AlGaN/GaN heterojunction. The p-type layer effectively depletes the 2DEG when $V_{GS} = 0$, resulting in a normally-off device. This approach is known as *e-GaN*.

2. **Cascode Configuration**: The use of a cascode pair, which includes a d-mode GaN HEMT and a low-voltage silicon MOSFET (Si MOSFET). The Si MOSFET controls the ON/OFF state of the combined device, while the GaN HEMT offers high voltage capability and low R_{ON}.

Similarly, the ***Vertical GaN (v-GaN)*** structure enables the achievement of high breakdown voltage and low on-resistance, as illustrated in the current aperture vertical electron transistor (CAVET – Current Aperture Vertical Electron Transistor) in Figure 4.4.

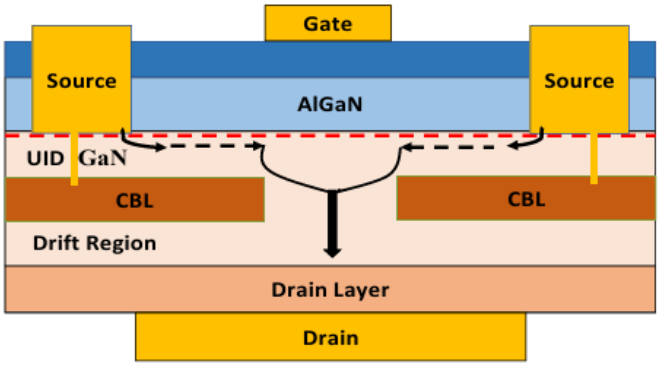


Figure 4.4: A typical vertical CAVET AlGaN/GaN HEMT structure.[9]

In this structure, the drain is located at the bottom, while the gate and source are on the top side of the device. The current flow is controlled by the gate through an aperture among the current blocking layers (CBLs – Current Blocking Layers) toward the drain. The current may flow through a large volume of material, which is typically achieved either by isolation implantation or by creating a p-type region in the GaN layer. Vertical devices utilize the bulk volume of the material and maintain the blocking voltage in the vertical direction, resulting in a reduced chip area for a given operating current. At present, bulk GaN substrates are not available in sizes larger than 100 mm, resulting in a significant increase in the cost of vertical GaN devices. However, the ability to operate at higher frequencies, as well as the improved efficiency of v-GaN power converters, will play a crucial role in the broader adoption of this emerging technology in the future.

4.2.3 Cascode GaN HMTs

In a ***cascode structure***, a high-voltage d-mode GaN HEMT and a low-voltage Si MOSFET are packaged together in order to achieve enhancement mode operation, as shown in Figure 4.5.

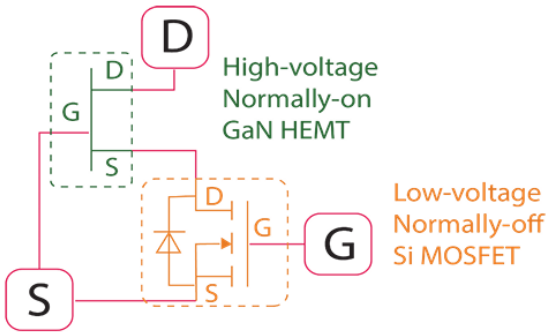


Figure 4.5: A typical cascode AlGaN/GaN HEMT normally-off structure.[9]

The primary function of the Si MOSFET is to switch the GaN HEMT on and off, with minimal increase in either on-resistance (R_{ON}) or reverse recovery charge (Q_{RR}). When the Si MOSFET has a relatively low R_{ON} compared to the GaN HEMT, the cascode configuration operates with high efficiency. The efficiency and thermal performance of cascode devices are comparable to those of e-GaN devices.

The cascode structure incorporates the reliable and robust silicon dielectric gate, which is compatible with standard, low-cost gate driver ICs. Cascode GaN HEMTs are widely used in high-voltage, high-current, and high-power applications, such as automotive systems. These devices are typically available for voltage ratings up to 600 V.

4.3 Advantages and Disadvantages of GaN HEMTs

One of the most significant advantages of GaN HEMT devices is their excellent performance in high-frequency applications. This is primarily due to the *high electron mobility* in GaN materials. Electrons move faster and more easily, allowing for quicker processing of electronic signals with lower losses. Additionally, GaN devices are efficient and capable of operating stably even at elevated temperatures. The *wide band gap* of GaN requires a higher temperature for thermal excitation, which makes it difficult for electrons to transition from the valence band

to the conduction band under the influence of an electric field. As a result, GaN devices exhibit *high breakdown field strength* and can withstand higher electric fields compared to conventional semiconductors.

Another important characteristic of GaN HEMTs is their *high thermal conductivity*, which enables efficient heat dissipation under high load conditions. Heat dissipation can also be achieved using fewer materials or cooling mechanisms, thus reducing the overall cost. Consequently, GaN-based devices demonstrate excellent performance and reliability in high-frequency, high-temperature, and high-voltage applications.

On the other hand, there are certain drawbacks to GaN HEMT devices. The most prominent disadvantages are the significantly higher cost and the complexity of the fabrication process. Compared to silicon-based devices, the manufacturing cost of GaN HEMTs is substantially higher. Silicon is a widely available material with mature fabrication processes, resulting in low production costs. In contrast, the production of GaN devices involves much more complex techniques, including Hydride Vapor Phase Epitaxy (HVPE), Metal Organic Chemical Vapor Deposition (MOCVD), and Molecular Beam Epitaxy (MBE). All these methods require expensive equipment and entail high manufacturing costs, leading to reduced growth rates and limited scalability.

Finally, although GaN shows excellent performance in high-frequency applications, its performance in low-frequency domains is limited by inherent physical characteristics, such as its wide band gap. In many low-frequency applications, traditional silicon-based devices outperform their GaN counterparts.

4.4 Technological Applications of GaN HEMTs

4.4.1 GaN HEMTs in Charger Circuit

The continuous advancement in semiconductor technology and the growing demand for more efficient solutions have led to the widespread adoption of GaN HEMT devices in modern power applications. One of their most prominent applications lies in power converters, such as

LCC converters used in lithium-ion battery charging circuits, as well as phase-shift full-bridge converters employed in electric vehicle chargers. In these systems, GaN devices demonstrate superior performance compared to conventional Si MOSFETs.

Furthermore, GaN HEMTs are effectively used in high-efficiency power supplies, power systems for telecommunications, DC-DC and AC-DC converters, as well as inverter circuits for photovoltaic and industrial applications. In such scenarios, their ability to operate efficiently at high frequencies and voltages plays a crucial role.

It is also important to highlight the growing use of GaN devices in mobile phone chargers, where they are gradually replacing silicon-based devices. GaN-based chargers are more compact in size and offer faster charging along with improved thermal performance.

4.4.2 GaN HEMTs in LiDAR Driver

LiDAR is a technology derived from radar and operates within the optical portion of the electromagnetic spectrum. In a typical setup, the light emitted into the atmosphere or space is reflected and then captured by the system after having interacted with one or more targets located at a specific distance from the LiDAR device. The adoption of LiDAR technology is expanding rapidly in modern times, particularly in autonomous driving systems, where it is used for the precise detection and mapping of the surrounding environment.

There are two primary measurement methods used in LiDAR applications:

1. **Direct Time of Flight (DToF):** Involves the direct measurement of the time of flight of a pulsed laser signal.
2. **Indirect Time of Flight (IToF):** Measures the phase difference of the signal based on the Doppler effect.

LiDAR applications require the use of pulsed laser driver circuits capable of delivering pulses with high peak current and very short rise and fall times. Compared to traditional silicon-based components, GaN HEMT devices offer superior performance and greater tolerance to high voltages.

4.4.3 GaN HEMTs in Aerospace

As previously mentioned, the highly significant characteristics of GaN HEMTs have naturally led to their utilization in satellite communication and navigation applications in space. GaN devices enable operation across various frequency bands, such as the P/L/S bands for communication and navigation satellites, as well as the X-band for deep space exploration and Earth observation applications. RF power amplifiers based on GaN technology provide high output power, improved efficiency, and a wider bandwidth compared to conventional technologies like GaAs-based amplifiers. GaN HEMT devices are specifically engineered to ensure reliability in space missions, and thanks to their inherent radiation hardness, they meet the demanding requirements of aerospace environments.

4.5 Comparison Between MOSFET and HEMT Technology

With technological advancements, semiconductor materials are entering the era of third-generation semiconductors. This category is dominated by wide bandgap materials, such as silicon carbide (SiC) and gallium nitride (GaN). SiC is the primary material used in the fabrication of power devices such as MOSFETs and IGBTs, while GaN is implemented in HEMT components. Characteristics such as low conduction resistance, high switching speed, and wide operational temperature range contribute to the replacement of Si IGBTs by SiC MOSFETs. However, GaN MOSFETs also demonstrate high potential as power switches due to their low energy losses. Third-generation semiconductors offer significant performance advantages over previous generations and hold promising prospects for future development.

4.5.1 Parasitic Capacitances and Operation Speed

In conventional silicon-based MOSFETs, the capacitances between the gate-drain (C_{gd}) and gate-source (C_{gs}) terminals are relatively high due to their planar structure and the inherent material limitations of silicon. These parasitic capacitances hinder the ability of the device to operate efficiently at high frequencies with minimal energy losses.

On the other hand, GaN HEMT devices exhibit exceptionally low input and output capacitances, facilitated by the high electron mobility achieved through the formation of a two-dimensional electron gas (2DEG). This characteristic is responsible for minimizing switching losses and enables operation at significantly higher frequencies. As a result, GaN HEMTs are ideal for applications in radio frequency (RF) and fast power conversion systems.

Moreover, MOSFETs experience switching delays during the turn-off phase due to the presence of reverse recovery charge. In contrast, systems designed with GaN HEMTs are more compact, offer higher power density, and demonstrate enhanced overall efficiency.

4.5.2 Operation in high and cryogenic temperatures

GaN HEMT devices demonstrate exceptional thermal stability, operating reliably at temperatures up to $300\,^{\circ}\mathrm{C}$ and remaining fully functional at cryogenic levels down to $77\,\mathrm{K}$ ($-196\,^{\circ}\mathrm{C}$). This resilience is primarily attributed to their wide bandgap (approximately 3.4 eV), which ensures consistent behavior in terms of threshold voltage, conduction resistance, and leakage losses, even in extreme environments. As such, GaN HEMTs are ideal for applications such as space radiation systems, where performance stability under thermal stress is critical.

In contrast, conventional bulk silicon MOSFETs are limited to a temperature range of approximately $-55\,^{\circ}\mathrm{C}$ to $150\,^{\circ}\mathrm{C}$. Beyond this range, their performance becomes unstable, with substantial power losses. These limitations stem from increased leakage current, the occurrence of latch-up, threshold voltage shifts, and other thermally-induced phenomena that affect their reliability.

Overall, while GaN HEMTs dominate in high thermal stress environments and high-frequency applications, MOSFET technology continues to play a vital role in advanced cryogenic and high-temperature systems. Its maturity, design flexibility, and continuous evolution across a wide temperature spectrum sustain its relevance in modern electronic systems.

Chapter 5

Design of Low Noise Amplifier Using 150nm GaN HEMT Technology

5.1 GH15LNF Technology Performance and Environment

The GH15-1x technology is based on AlGaN/GaN high electron mobility transistors (HEMTs) with a gate length of 150 nm and a slanted gate-foot profile. Two FET topologies are available: one with source-terminated field plates, and another without a field plate, targeted for switch applications. Two metallization layers are used for interconnects, MIM-capacitors, high-frequency transmission lines, and inductors. The second metallization layer also provides air bridges, enabling topological flexibility and the ability to cross underlying structures with low parasitic capacitance. Additionally, two types of thin-film resistors are available. This technology is particularly suited for the design of monolithically integrated, robust, low-power MMICs, as well as multi-stage high-power and high-efficiency amplifiers operating at frequencies up to 35 GHz.

As part of the present study, the linear model **GH15LNF** was utilized. This model is a variant of the **GH15** technology developed by **UMS** and is specifically designed for low-noise amplifier (**LNA**) applications. It is based on **GaN-on-SiC** technology with a gate length of **0.15** μ**m** and offers excellent performance at high frequencies.

The design environment used in this project for the design of a Low Noise Amplifier at 5GHz is the AWR Design Environment by Cadence. AWR is a software that provides advanced tools for the design and analysis of RF circuits.

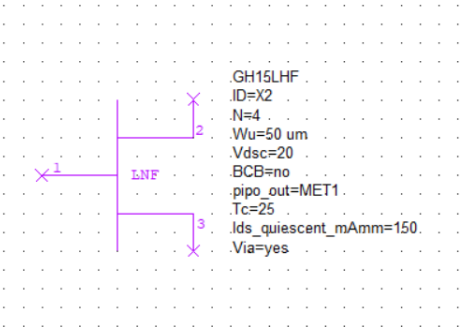


Figure 5.1: Linear noise model view and parameters

5.2 Schematic Design Methodology

5.2.1 Device Characterization for Bias Point Optimization

It is essential to thoroughly analyze the behavior of the selected device before initiating the amplifier design process. For this purpose, the circuit shown in Figure 5.2 was implemented to observe the most critical measurements that influence the design of a low-noise amplifier. The frequency of interest is **5 GHz**, aiming at the design of a **narrowband LNA**.

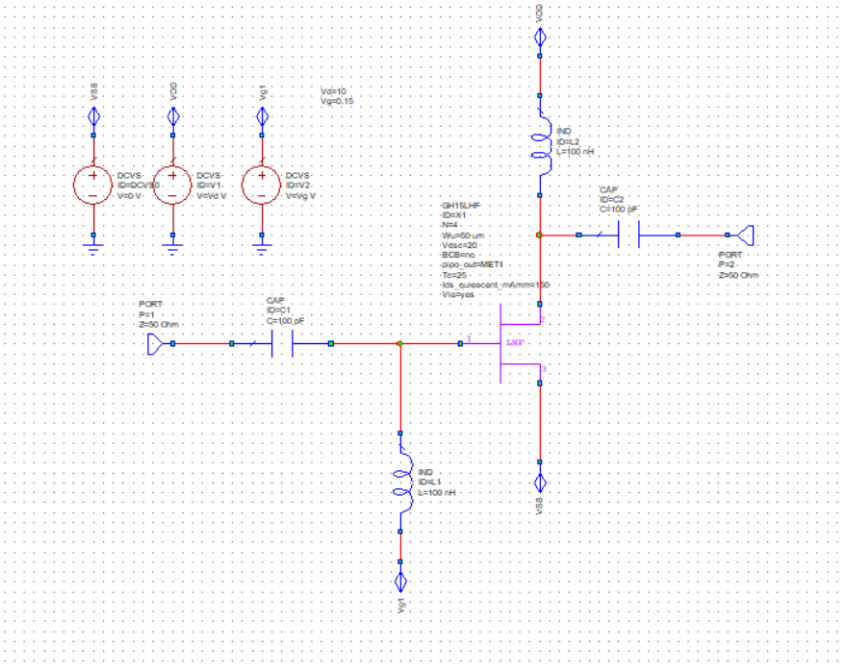


Figure 5.2: Basic circuit for transistor characterization.

I_D vs. V_D

The initial step involved observing the I_D *vs.* V_D measurements, where the drain current is

plotted on the vertical axis and the drain voltage on the horizontal axis. Each curve in the diagram corresponds to a different value of the gate voltage V_G, which was varied using the `SWPVAR` function in AWR to capture all possible cases.

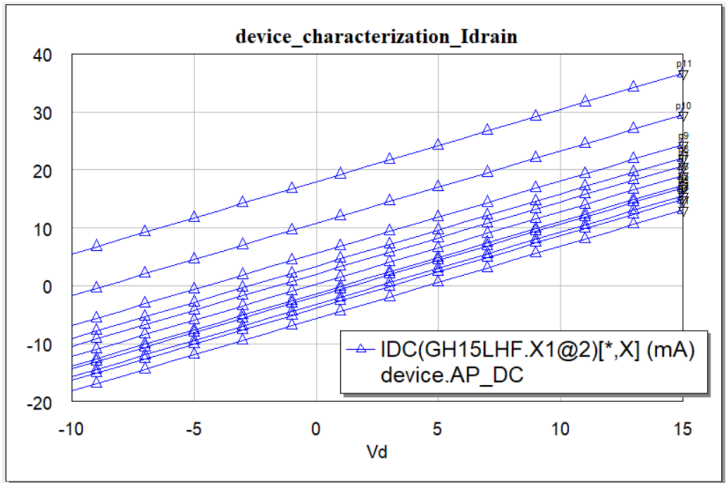


Figure 5.3: Drain Current vs. Drain Voltage Characteristic Curves.

This type of analysis is referred to as a **DC simulation** and is performed to determine the optimal bias point of the transistor. Figure 5.3 illustrates the saturation region of the transistor, within which its behavior is examined to define an appropriate operating point. Based on the results, it is observed that for a gate voltage of $V_{\text{Gate}} = 0.15\,\text{V}$ and a drain voltage of $V_{\text{Drain}} = 10\,\text{V}$, the device delivers a drain current of approximately $I_{\text{Drain}} \approx 23\,\text{mA}$. This particular bias point was selected because it offers relatively low current consumption, and the drain voltage $V_{\text{Drain}} = 10\,\text{V}$ remains well below the device's breakdown voltage.

Although GaN devices typically feature a high breakdown voltage (around 20 V), the operating voltage was conservatively limited to ensure device safety. Another contributing factor to this decision is the lack of provided lifetime data for GaN devices in this technology. Consequently, lifetime-related simulations could not be performed within the AWR environment. As such, a more conservative bias point was chosen to avoid subjecting the device to stress or operating it near its physical limits.

In Figure 5.4, the ideal I–V characteristics of a MOSFET are illustrated. Additionally, the three main operating regions of a transistor are annotated: the **Cut-Off Region**, the **Linear (Triode) Region**, and the **Saturation Region**. The *Cut-Off Region* occurs when the gate-to-source voltage is lower than the threshold voltage ($V_{GS} < V_{th}$), resulting in the transistor being turned off and no drain current flowing. The *Linear Region* lies to the left of the red

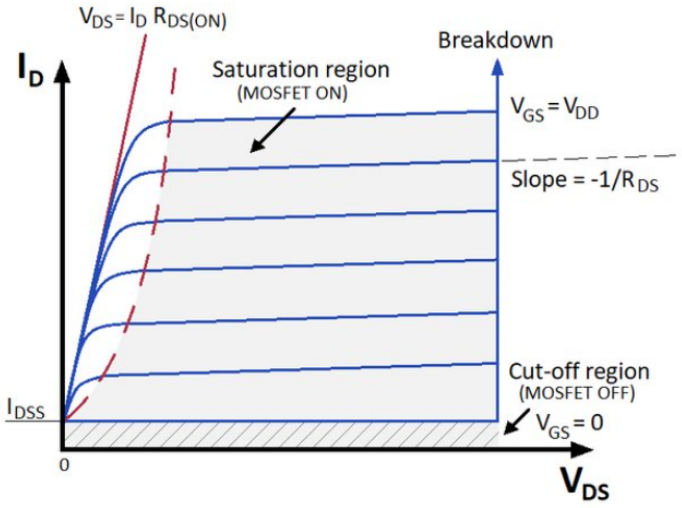


Figure 5.4: Regions of the FET transistor on the IV Characteristic Curves.[11]

dashed line in the diagram. Beyond this boundary, the *Saturation Region* begins, where the device operates as a current amplifier. This region is defined by the condition $V_{DS} \geq V_{GS} - V_{th}$.

It is evident that Figure 5.3 illustrates the transistor's behavior in the saturation region, ranging from the *knee voltage* (V_{knee}) up to the *breakdown voltage* (V_{BR}).

Another important phenomenon observable in a transistor is the **Early effect**. Ideally, in the saturation region, the drain current (I_D) should remain constant and independent of the drain voltage (V_D). However, in practice, I_D slightly increases with V_D even in saturation. As a result, the characteristic curves exhibit a small positive slope. If these curves are extended backward, they intersect the V_D axis at a common point, as shown in Figure 5.5. This point is defined as the **Early voltage** (V_A). The higher the value of V_A, the better the transistor's linearity and overall performance.

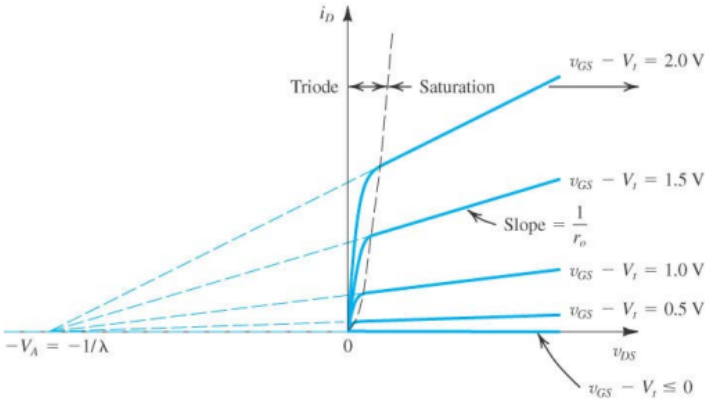


Figure 5.5: The effect of V_D on I_D in the saturation. region[12]

It should also be noted that the model used, `GH15LNF`, is a linear model. Therefore, it is specifically designed for simplified RF simulations centered around a fixed bias point, rather than fully nonlinear transistor behavior.

Figure 5.6 illustrates the drain current as a function of gate voltage for a fixed drain voltage of 10 V, with the selected bias point clearly marked using a marker for reference.

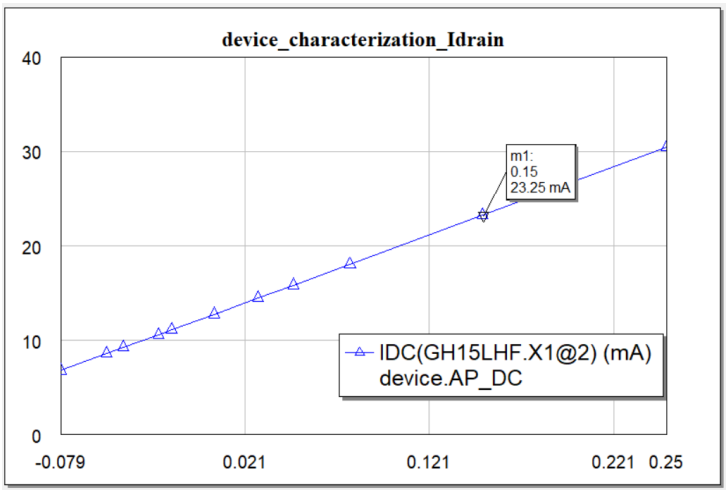


Figure 5.6: Drain Current vs. Gate Voltage at $V_{Drain} = 10\,\text{V}$.

Device Noise Figure

The NF diagram illustrates the behavior of the amplifier with respect to the additional noise introduced into the signal during the amplification process. For the design of an efficient LNA, especially in RF applications, minimizing noise is a critical factor. Therefore, to evaluate the performance of the low noise amplifier, a noise figure analysis was conducted, as shown in Figure 5.7. The diagram confirms that the device maintains low values for both NF and NF_min, indicating that it is suitable for use in the design of an LNA.

Device Maximum Gain

In addition to the NF, another key performance indicator of an LNA is the amplifier's gain. At this point, the gain diagram was examined, shown in Figure 5.8, for the operating frequency of 5 GHz. Based on the results, it was observed that the amplifier provides a sufficiently high gain while maintaining a low noise level.

Device Stability

In amplifiers, stability is a fundamental requirement that ensures reliable operation under all conditions. Figure 5.9 illustrates the tendency of the circuit to exhibit unwanted oscillations.

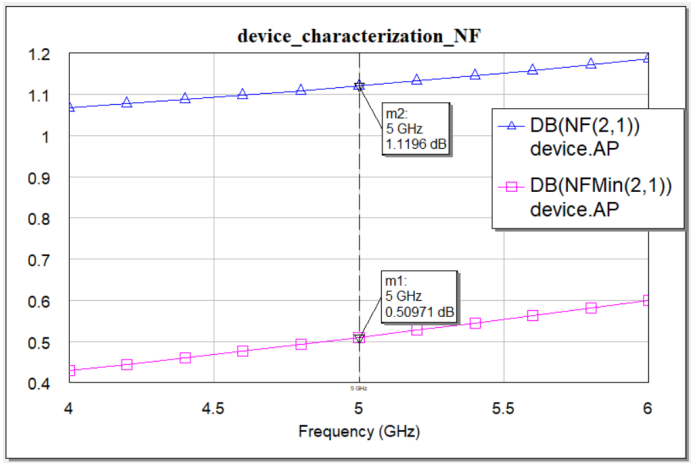


Figure 5.7: NF and NF_min Curves.

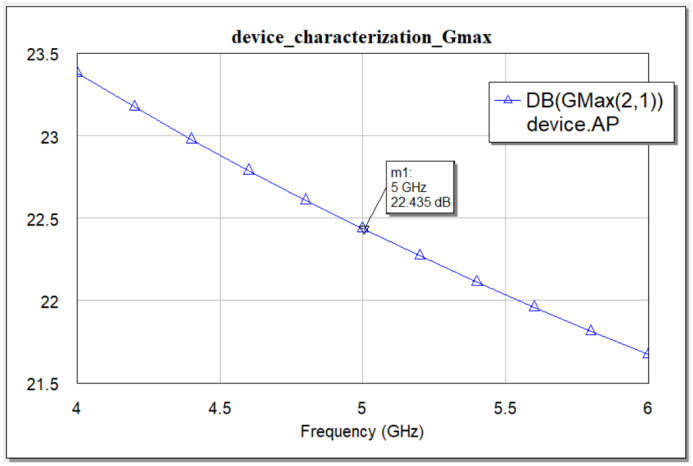


Figure 5.8: Maximum Gain Curve.

During the analysis, parameters such as the Rollet stability factor K and the determinant Δ were used. The results show that the device remains nearly stable at the 5 GHz frequency. This occurs because the K factor should be greater than unity, which could not be achieved with this particular device. However, this is not considered a critical issue, as additional components are typically introduced during the LNA design process to stabilize the circuit and ensure reliable amplifier performance.

5.2.2 Core Design Strategy for LNAs

In this project, which focuses on the development of a low-noise amplifier (LNA) operating at **5 GHz**, the design methodology and fundamental steps were inspired by the approach described in the article *"Algorithmic Design of CMOS LNAs and PAs for 60-GHz Radio"*. This article provides a detailed methodology for architectural selection, bias point definition,

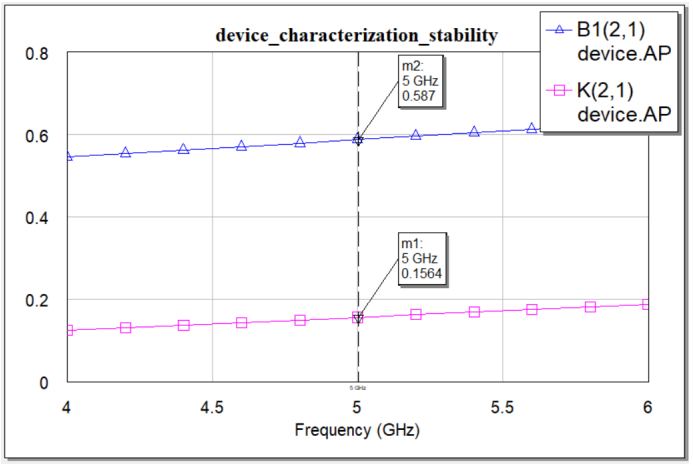


Figure 5.9: Stability Factors

and performance optimization, and therefore served as a critical starting point for the design presented in this work.

It is also important to highlight that the **cascode topology** was selected as the most appropriate architecture. This topology enables the achievement of high gain, improved input–output isolation, and enhanced stability, all of which are essential for an efficient LNA design. Moreover, it contributes to the suppression of the Miller effect, which is beneficial for broadband performance. However, in the current design environment, this topology requires the separation of the cascode stages, since only linear transistor models are provided by the PDK. This separation may lead to an increase in both the silicon area and power consumption when compared to a simpler common-source configuration.

The design process begins with the definition of the key LNA parameters, based on a set of predefined specifications inspired by those described in the aforementioned paper. The primary performance metrics under consideration include noise figure (NF), gain, linearity, and amplifier bandwidth at the specified operating frequency. The chapter concludes with a comparative evaluation of the proposed design against other related works in the literature.

The design methodology employed in this study is summarized in six fundamental steps. By following this methodology, optimal noise performance is achieved within the constraints of the selected technology. The steps undertaken and their detailed analysis are presented below.

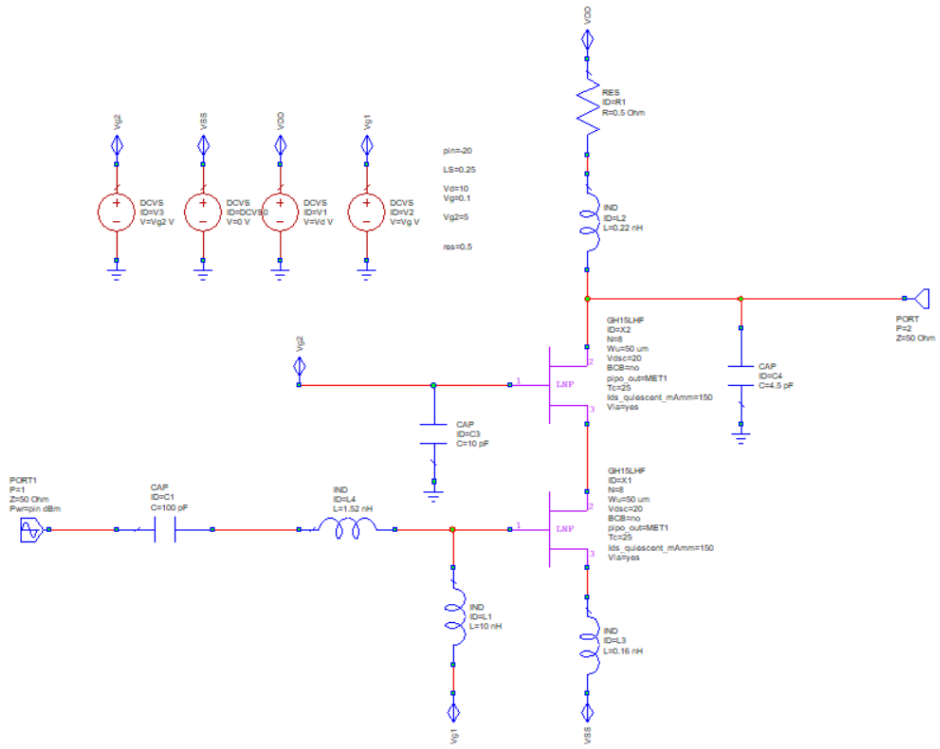


Figure 5.10: Cascode Common Source LNA Schematic - the basis for this design.

5.2.3 Step 1: Biasing for Minimum Noise Figure

Following the adopted methodology, the first step involves biasing the transistor at the optimal current density (J_{opt}), aiming to minimize the transistor's noise figure (NF_{min}). As shown in Table 5.1, the gate voltage V_{gate} was set accordingly, along with the fundamental device parameters. At this stage of the design, the width of the device does not significantly affect the performance, as the key objective is to determine the appropriate bias point, which mainly depends on current density.

Table 5.1: Device Characteristics and Gate Bias Voltage

Parameter Description
Gate bias voltage V_{gate} = 0.1 V
Drain voltage V_{drain} = 10 V
Finger Width = 50 μm
Number of fingers = 8

5.2.4 Step 2: Optimal Finger Width for Minimum Noise Figure and Maximum Gain

In this step, the optimal Finger Width (W_f) must be determined in order to minimize the noise figure (NF_{min}) and maximize the amplifier gain (G_{max}). The circuit is biased with a gate voltage of $V_{\text{gate}} = 0.1\,\text{V}$, corresponding to the minimum noise level identified in the first step.

To determine W_f, a new SP analysis is performed, in which the Number of Fingers (NoF) is varied using the SWPVAR function, taking values from the set $\{2, 4, 6, 8, 10, 12\}$, in accordance with the noise parameters of the GH15-1x device for the linear noise model employed.

By varying NoF while keeping the total gate width constant, W_f is calculated using the following relation:

$$W_f = \frac{\text{Total Gate Width}}{\text{NoF}} = \frac{400\,\mu\text{m}}{8} = 50\,\mu\text{m} \tag{5.1}$$

From the plots in Figure 5.11 (for NF_{min}) and Figure 5.12 (for G_{max}), it is evident that increasing the number of fingers results in both a reduction of the noise figure and an increase in gain. However, after careful evaluation, a choice of 8 fingers is considered prudent and reliable for the design, also remaining within the GH15LNF noise capability validation domain relevant to the model under investigation.

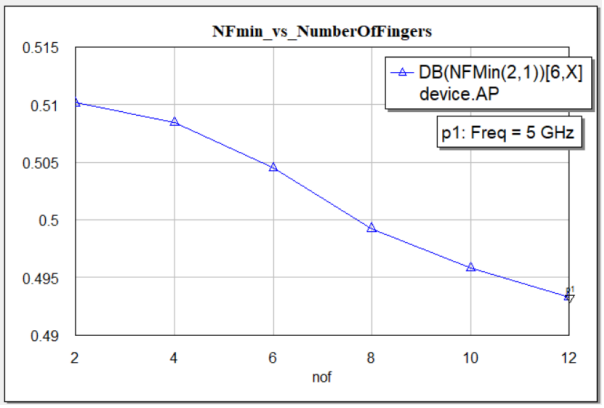


Figure 5.11: Graph of NF_{min} as a function of Number of Fingers.

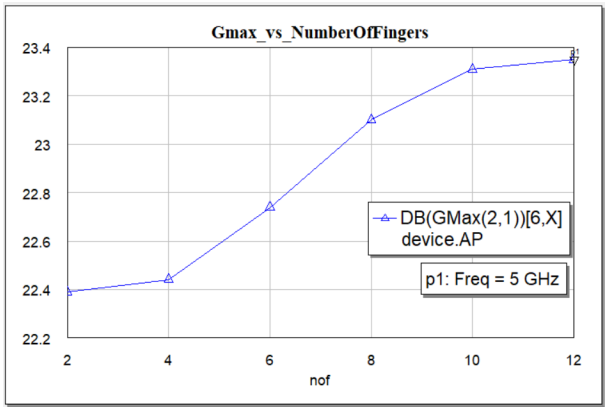


Figure 5.12: Graph of $G_{\max}$ as a function of Number of Fingers.

5.2.5 Step 3: Inductive Degeneration Technique

According to this technique, an inductor is placed in series with the transistor source, as illustrated in Figure 5.13. This improves input matching and reduces noise without significantly compromising gain. The addition of the inductor increases the real part of the input impedance, thereby allowing the input to be matched to $50\,\Omega$. Simultaneously, linearity is enhanced, noise is reduced, and the amplifier's stability is improved.

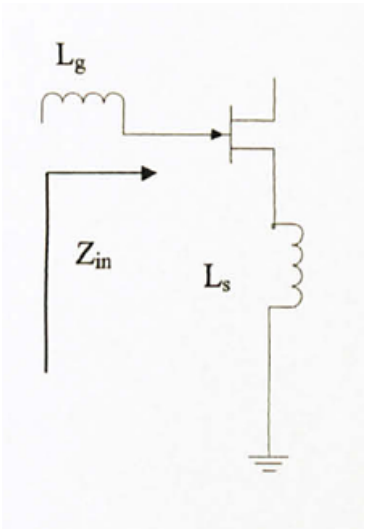


Figure 5.13: Implementation of Inductive Degeneration.[13]

Input Matching Strategy Based on Small-Signal Modeling

In Figure 5.14, the Z-Smith Chart is plotted for the reflection coefficient S_{11}, after achieving input matching. In order to make the real part of the input impedance equal to $50\,\Omega$, a parameter sweep was performed for the value of L_s, which was ultimately set to 0.32 nH.

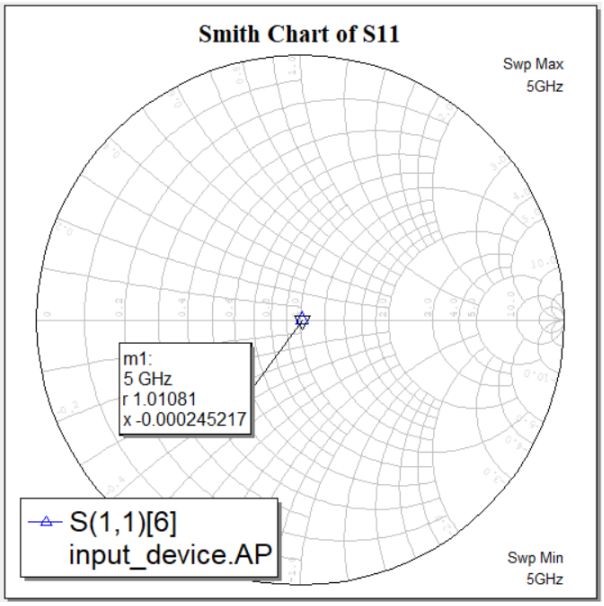


Figure 5.14: Input Matching with Inductive Degeneration.

An initial estimation for the value of L_s was made theoretically, based on the small-signal model derived from the circuit analysis, as shown in Figure 5.15.

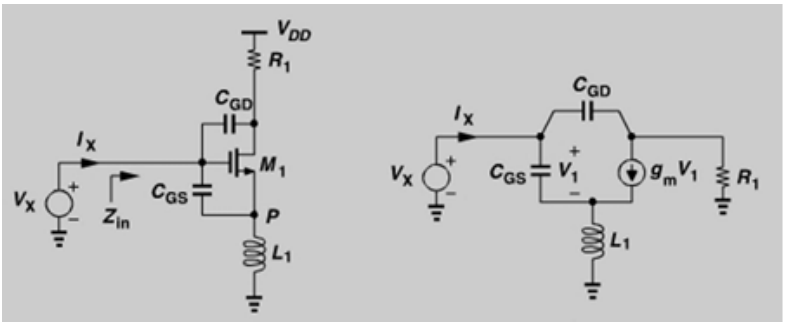


Figure 5.15: Small-Signal Equivalent Circuit.[7]

The small-signal analysis of the circuit is presented below. The aim of the circuit is to provide an input impedance Z_{in} of $50\,\Omega$ with zero imaginary part, which is stable and frequency-independent. If the parasitic capacitances C_{GD} and C_{SB} of the transistor are neglected, the input current I_X entirely flows through the gate-source capacitance C_{GS1}, resulting in a gate-source voltage:

$$V_{\text{GS}} = \frac{I_X}{C_{\text{GS1}} \cdot s} \tag{5.2}$$

Consequently, the drain current generated by the controlled current source is:

$$g_m V_{\text{GS}} = \frac{g_m I_X}{C_{\text{GS1}} \cdot s} \tag{5.3}$$

These two currents flow through the degeneration inductor L_S, resulting in a voltage:

$$V_P = \left(I_X + \frac{g_m I_X}{C_{\text{GS1}} \cdot s} \right) \cdot L_S \cdot s \tag{5.4}$$

Since the total input voltage is:

$$V_X = V_{\text{GS1}} + V_P \tag{5.5}$$

the input impedance becomes:

$$Z_{\text{in}} = \frac{V_X}{I_X} = \frac{1}{C_{\text{GS1}} \cdot s} + L_S \cdot s + \frac{g_m L_S}{C_{\text{GS1}} \cdot s} \tag{5.6}$$

However, when the gate-drain parasitic capacitance C_{GD1} is also considered in the analysis, the input impedance takes the following more complex form:

$$Z_{\text{in}} = \frac{1}{C_{\text{GS1}} \cdot s} + L_S \cdot s + \frac{g_m L_S}{C_{\text{GS1}} \cdot s} \left[1 - \frac{2C_{\text{GD1}}}{C_{\text{GS1}}} - L_S C_{\text{GD1}} s^2 - \left(R_1 C_{\text{GD1}} + g_m L_S \cdot \frac{C_{\text{GD1}}}{C_{\text{GS1}}} \right) s \right] \tag{5.7}$$

To overcome this issue, an inductor L_G is introduced at the gate input. Thus, the input impedance is calculated as:

$$Z_{\text{in}} = \frac{1}{C_{\text{GS1}} \cdot s} + (L_S + L_G) \cdot s + \frac{g_m L_S}{C_{\text{GS1}} \cdot s} \tag{5.8}$$

which simplifies to the compact form:

$$Z_{\text{in}} = \frac{g_m L_S}{C_{gs}} + j \left[\omega (L_G + L_S) - \frac{1}{\omega C_{gs}} \right] \tag{5.9}$$

Multiplicity Constraints

After establishing the gate bias voltage at $V_{\text{gate}} = 0.1\,\text{V}$ and setting the number of fingers to 8, the third step involves determining the appropriate multiplier value that corresponds to the actual impedance $Z_{\text{opt}} = 50\,\Omega$ at the operating frequency. At this stage, the device was modified accordingly by introducing a variable named `mult` to increase the number of device instances.

However, it was observed that as the multiplier increased, the minimum noise figure (NF_{min}) also exhibited a dramatic increase. This behavior is attributed to the nature of the `GH15LNF` model, which functions as a compact low-noise model. Specifically, it is developed to represent the behavior of a single core finger element and does not support parameterization via the multiplier. The use of a multiplier leads to an unrealistic simulation because it fails to account for parallelization effects, such as the increase in parasitic components and the distribution of noise.

Therefore, to ensure simulation accuracy and the reliability of results, the `GH15LNF` model must be used only in configurations where no multiplier is applied. Instead, scaling should be achieved by increasing the number of fingers (*Number of Fingers*), rather than by parallelizing through a multiplier.

5.2.6 Step 4: Addition of L_G for Input Matching Tuning

As discussed in Step 3, the addition of the inductor L_G at the gate input results in a simplified expression for the input impedance Z_{in}, as shown in Equation (5.9). This simplification facilitates the selection of suitable values for the inductors L_G and L_S, based on the known parameters g_m and C_{gs}, in order to achieve an input impedance of $50\,\Omega$.

Therefore, based on the aforementioned expression, an initial estimation of the values for L_G and L_S can be obtained as follows:

$$\text{Real Part:} \quad \frac{g_m L_s}{c_{gs}} = 50\,\Omega \quad \Rightarrow \quad L_s = \frac{50\,c_{gs}}{g_m} \tag{5.10}$$

$$\text{Imaginary Part:} \quad \omega(L_G + L_s) - \frac{1}{\omega c_{gs}} = 0 \quad \Rightarrow \quad L_G = \frac{1}{\omega^2 c_{gs}} - L_s \tag{5.11}$$

These estimations for the inductors L_G and L_S can serve as initial values, which may require further tuning to precisely achieve an input impedance $Z_{\text{in}} = 50\,\Omega$.

In conclusion, the inclusion of the inductor L_G at the gate input is a key technique for optimizing both the input matching and the noise performance of the LNA. Specifically, it

compensates for the imaginary part of the input impedance introduced by the gate-source capacitance C_{gs}, enabling resonance at the desired operating point. Additionally, this resonance enhances the amplifier's performance at the target operating frequency.

Inductive Peaking Technique

The addition of the inductor L_G not only cancels out the imaginary part of the input impedance—bringing it close to zero—but also introduces an additional benefit: it provides passive gain at the gate terminal of the device. This gain is illustrated in Figure 5.16, which shows the AC gain at the gate terminal. As observed, the curve exhibits a pronounced peaking at the operating frequency, justifying the chosen value of L_G. The resulting passive gain is approximately 1.5 dB, which significantly contributes to the overall gain of the amplifier.

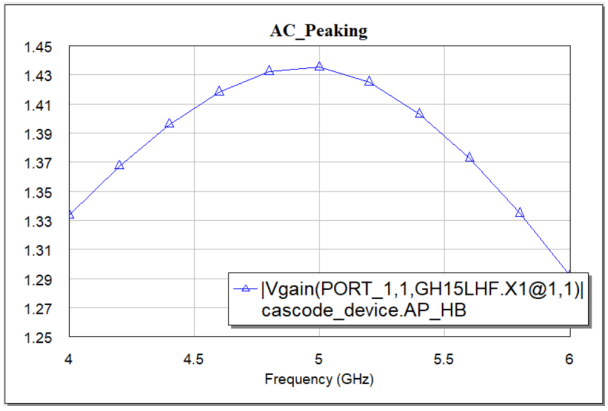


Figure 5.16: AC Gain Peaking

5.2.7 Step 5: Scale the Size of the Cascode Device

At this stage, having already determined suitable values for the inductors L_G and L_S to achieve input matching, and having defined the sizing for the device in the common-source stage, the dimensions of the cascode device are now calculated for the implementation of the chosen topology.

To simplify the design and maintain circuit symmetry, the cascode transistor is chosen to be identical to the one used in the common-source stage, employing the same number of fingers and finger width (W_f). This approach ensures consistency in parasitic capacitances and dynamic behavior between the two transistors, thereby promoting predictable and stable circuit performance.

Furthermore, an additional DC bias source is introduced to appropriately bias the cascode device. The value of this bias voltage is selected such that the current through the transistors remains as stable as possible, while the drain voltage of the cascode transistor is equally distributed across both active devices. Finally, due to the addition of the cascode stage, the overall drain supply voltage (V_{drain}) must be approximately doubled. This increase ensures that each transistor receives the same bias voltage as before, thereby preserving optimal operating conditions for both devices.

It is important to note that, in order to achieve maximum power transfer, the output impedance of the common-source device should be as close as possible to the input impedance of the cascode device. Furthermore, the proper sizing of the cascode device is critical not only for maintaining low noise but also for minimizing parasitic effects, particularly at high frequencies.

5.2.8 Step 6: Add Output Matching Network

The output matching network of the LNA is designed to ensure optimal power transfer from the amplifier's output stage to the subsequent stage or the antenna, as illustrated in Figure 5.17.

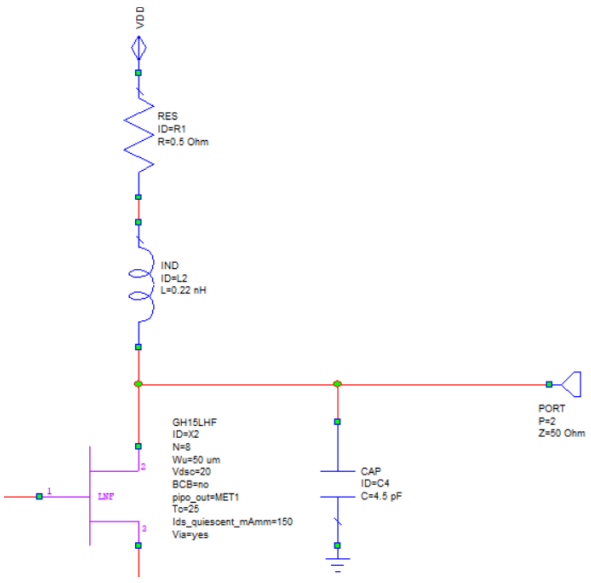


Figure 5.17: Output Matching Network Design.

An inductor is again used as the output load, benefiting from its low parasitic resistance which minimizes noise contribution. The inductor L_2 operates as part of the output network and simultaneously serves as an RF choke, allowing the DC bias current to flow for proper transistor

operation. A small resistor R_1 (0.5 Ω) is placed in series with the inductor to enhance circuit stability by lowering the quality factor Q of the resonant network, thus preventing possible oscillations. The parallel capacitor C_4 primarily acts as a DC block, isolating the output node from any DC components. Finally, the output network is designed to match a 50 Ω load, ensuring maximum power transfer and minimal reflections, thereby contributing to the overall stability and performance of the amplifier.

5.2.9 Design Validation and Results of the LNA

This section presents the final simulation results obtained upon completion of the LNA design, targeting operation at 5 GHz for 5G applications. The performance of the circuit is evaluated based on the design specifications and includes all key parameters such as gain, noise figure, input and output matching, as well as linearity and stability. All the diagrams shown below represent the behavior of the circuit before layout (pre-layout results).

Noise Figure (NF) and NF_{min}

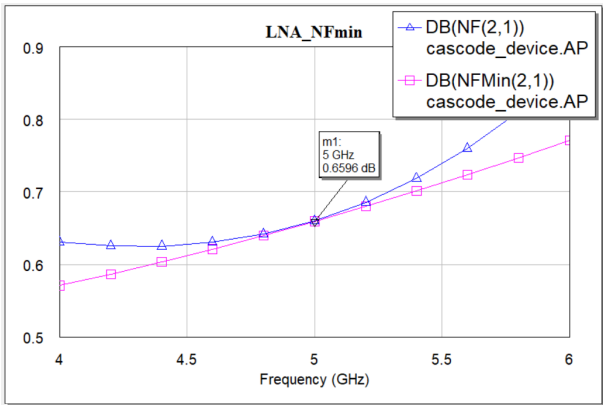


Figure 5.18: Noise Figure and minimum achievable noise figure (NF_{min}).

Figure 5.18 illustrates the noise figure (NF) and the theoretically minimum achievable noise figure (NF_{min}) as a function of frequency. As shown, the NF remains very low at the desired operating frequency, validating the LNA's high performance with respect to input noise.

S-parameters (S_{11} and S_{22})

At the target frequency, both the input (S_{11}) and output (S_{22}) reflection coefficients are below -10 dB, which indicates effective impedance matching and minimal signal reflections at

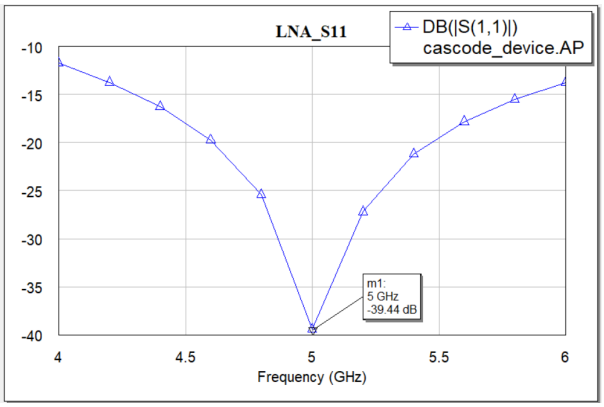


Figure 5.19: Input reflection coefficient S_{11}.

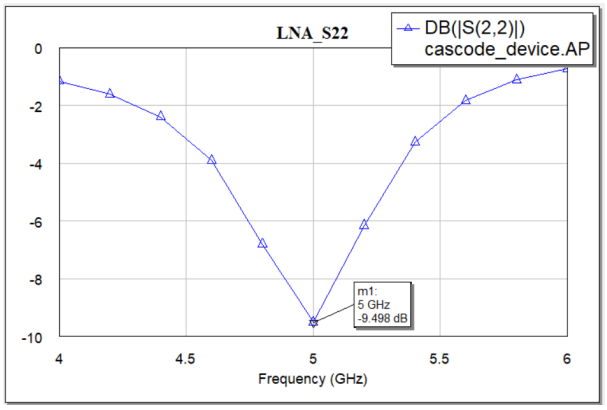


Figure 5.20: Output reflection coefficient S_{22}.

the amplifier's input and output ports.

Maximum Gain

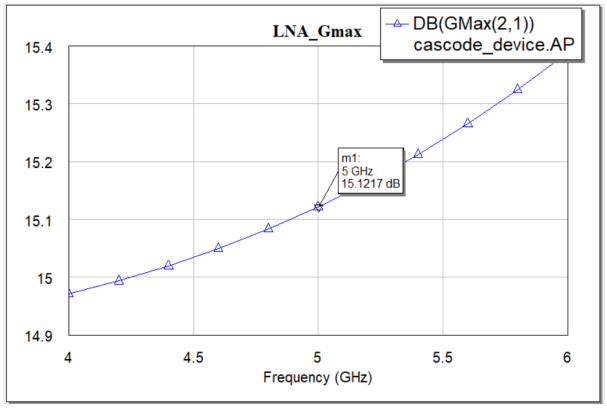


Figure 5.21: Maximum gain (G_{max}).

As shown in Figure 5.21, the gain curve exhibits a peak slightly above 15 dB at the frequency of interest. Although a higher gain could potentially be achieved—as suggested by the increasing slope of the curve—simulation tests showed that the maximum attainable gain at 5 GHz was 15.3 dB. However, in doing so, the minimum achievable noise figure (NF_{min}) increased by

approximately 0.15 dB. Given that noise performance is a critical factor in LNA design, the decision was made to prioritize maintaining a low NF_{min} at the expense of slightly lower gain.

Stability Factors (K, Δ)

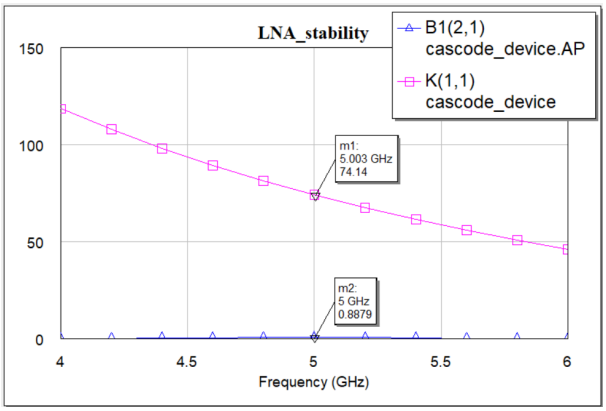


Figure 5.22: Stability factors K and Δ.

Figure 5.22 shows the stability factors K and Δ. As previously discussed in Chapter 3 (Section 3.1.6), a circuit is considered unconditionally stable if it satisfies the conditions $K > 1$ and $|\Delta| < 1$ across the entire frequency range. From the plot, it is evident that the proposed design meets these stability criteria, thereby ensuring unconditional stability of the amplifier throughout the band of interest.

5.3 Evaluation and Comparison with Other Works

Initially, Table 6.2 presents the final design parameters and values that were determined for the implementation of the proposed low-noise amplifier:

To thoroughly evaluate the effectiveness of the proposed design, it is essential to compare the results of this work with other published designs that utilize the same technology and operate at similar frequency ranges. Such a comparison allows for a comprehensive assessment of the amplifier's performance with respect to key metrics such as noise figure, gain, power consumption, and linearity. Accordingly, Table 5.3 provides a summary of the key performance metrics of this work alongside those of comparable designs, highlighting the advantages and unique characteristics of the proposed topology.

Table 5.2: Key Parameters of the LNA Transistor and Matching Network Elements

Desing Parameter	**Value**
1. V_{drain}	10 V
2. V_{gate}	0.1 V
3. Gate Length (L)	150 nm
4. Finger Width (W)	50 μm
5. Number of Fingers	8
6. Number of Multipliers	1
7. Gate (Series) Inductor	1.52 nH
8. Drain Inductor	0.22 nH
9. Source (Degeneration) Inductor	0.16 nH

Table 5.3: Comparison with Other Works

Technical Comparison Between Existing GaN LNA Designs							
Parameter	**[27]**	**[28]**	**[29]**	**[30]**	**[31]**	**[23]**	**This Work**
Process	GaN-HEMT	0.25μm GaN	0.13μm CMOS	90 nm RF-SOI	0.5 μm GaAs pHEMT	GaN-HEMT	**GaN-HEMT**
Frequency (GHz)	3.5	5-6	3-7	5	2.5-5	3.5	**5**
Structure	CS	3-STAGE CS with FB	Cascode CS-CG without FB	CS with resistive FB	CS with FB	CS with Inductive Degeneration	**Cascode CS-CG**
NF (dB)	1.232	5.5	2	1.73	2.6	1.2	**0.65**
Gain (dB)	16.225	12	20	19.9	17	7.2	**15.12**
P1dB (dBm)	NA	NA	NA	NA	2.3	NA	NA
IP3 (dBm)	NA	NA	NA	-15.4	-2	NA	NA
S_{11} **(dB)**	–23.785	NA	–10.5	–9.4	NA	-14.4	**-39.44**
S_{22} **(dB)**	–23.516	NA	–5.4	–15	NA	-15.5	**-9.49**

Chapter 6

Design and Simulation of Low Noise Amplifier in 22FDX Technology

6.1 SOI Technology and Cadence Environment

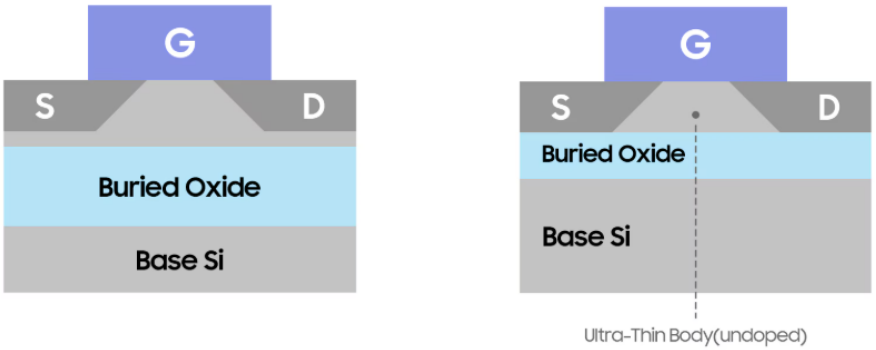
The rapid advancement of SOI CMOS technology is attributed to its ability to address the fundamental challenges encountered in bulk silicon CMOS, particularly in the downscaling of MOSFETs to nanometer dimensions. In the late 1990s, substrate technology entered a dynamic phase with the industry's transition to SOI wafers. SOI substrates not only enabled an increase in drive current but also significantly reduced parasitic losses and capacitances. As a result, the integrated circuit industry was able to develop outstanding solutions for high-performance logic circuits using SOI technology. Applications and adoption of SOI expanded rapidly as SOI wafers became more accessible and cost-effective, thus penetrating mainstream ultra-large-scale integration (ULSI) circuits. Today, SOI technology has become a key platform for integrated circuit fabrication, ranging from high-performance processors to RF front-end modules (FEMs), securing its position in the ever-evolving landscape of electronic technology.

6.1.1 FDSOI vs PDSOI Technology

SOI MOSFETs are divided into two main categories with significant differences in their electrical properties, depending on the thickness and doping level of the buried oxide layer (BOX): the *Partially Depleted (PD)* and *Fully Depleted (FD)* SOI MOSFETs.

Partially Depleted (PD) SOI MOSFETs, also known as thick-film SOI transistors, feature a crystalline silicon layer with a typical thickness between 50–100 nm and a BOX thickness

ranging from 100–200 nm. Their structure is shown in Figure 6.1(a). The BOX plays a crucial role in limiting junction leakage currents and reducing parasitic capacitance between the source, drain, and body. A major drawback of this technology is the *floating body effect*, which arises due to the lack of a voltage bias at the substrate. Holes generated through hot-carrier effects become trapped in the body, leading to hysteresis, threshold voltage (V_{th}) fluctuations, and the so-called *kink effect*, characterized by a sudden increase in drain current under high drain bias. While mitigation techniques such as body grounding exist, their implementation is not always feasible in industrial processes. Nevertheless, PD-SOI technology offers excellent performance and electrical isolation, making it suitable for analog and power electronics applications.



(a) PD-SOI Structure (b) FD-SOI Structure

Figure 6.1: SOI MOSFET Structures: (a) PD-SOI, (b) FD-SOI.[14]

Fully Depleted (FD) SOI MOSFETs, also referred to as thin-film SOI transistors, are designed with a silicon layer thinner than the maximum depletion width (t_{Si} ¡ W_{dep}). Their structure is illustrated in Figure 6.1(b). In this configuration, the channel is fully depleted both below and above the threshold voltage, providing superior gate control. This allows for suppression of both the short-channel and floating-body effects, without the need for heavy doping. FD-SOI devices exhibit higher carrier mobility, lower leakage currents, and improved energy efficiency, while maintaining a simple planar 2D architecture, in contrast to more complex 3D technologies such as FinFETs and GAA. However, a primary limitation is the *self-heating effect*, attributed to the low thermal conductivity of the BOX, which can reduce performance under high-power operation. Despite this, FD-SOI is currently regarded as one of the most promising technologies for low-power, high-performance digital and RF applications.

6.2 Super Low VT - NFET FD SOI Technology Performance

A detailed analysis of the operation of the SOI transistor used in the design is considered particularly important. As mentioned in Section 5.2.1, this is the first essential step in evaluating the behavior of the device. The transistor employed in the design of the low-noise amplifier using SOI technology is the Super Low VT (SLVT) NFET, whose key parameters are summarized in Table 6.1.

Table 6.1: SLVT Design Parameters

SLVT Design Parameters	
Device Type	Super Low VT (SLVT) NFET
Library Name	`cmos22fdsoi_rf`
PDK Version	22FDX-EXT/V1.0_3.0
Gate Length	20 nm
Number of Fingers	8
Finger Width	2 μm

In Figure 6.2, the basic circuit used for the analysis of the key characteristics of the SLVT is shown, with the aim of determining its optimal bias point.

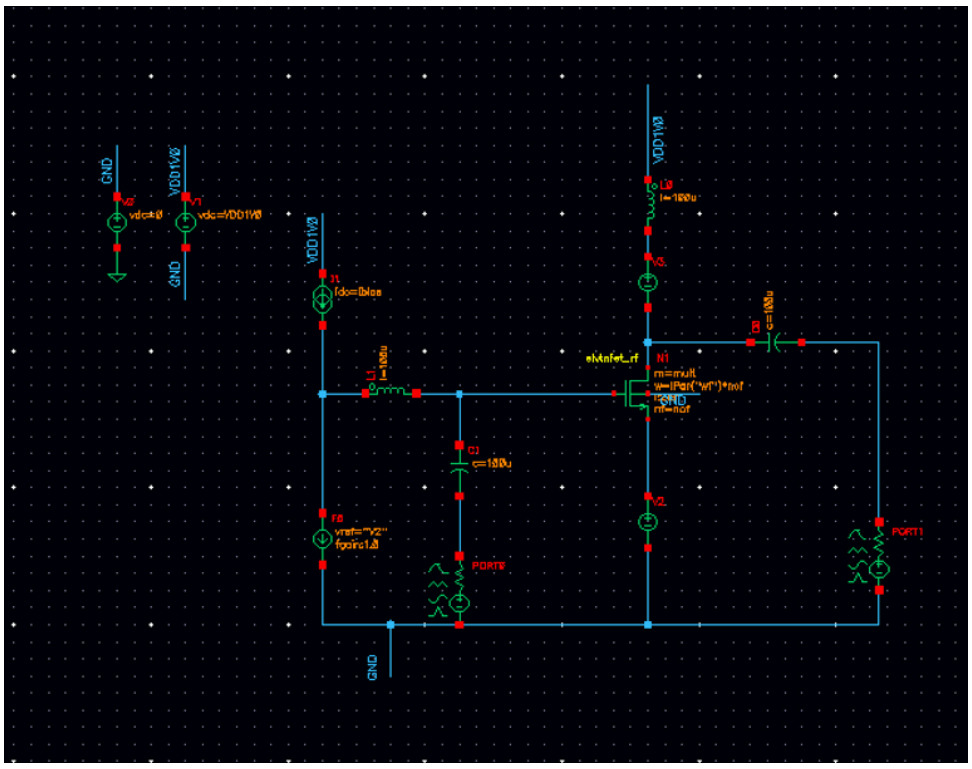


Figure 6.2: Basic circuit for device characterization

I_D vs. V_D

One of the most important initial measurements is the extraction of the I_D *vs.* V_D characteristics, which, along with the I_D *vs.* V_G curves and the transconductance g_m, are part of the DC analysis of the device. Figure 6.3 illustrates the plots obtained using a DC Sweep, where the drain voltage V_D was swept from 0 to 1 V in steps of 0.1 V. Simultaneously, the drain current I_D was swept from 1 mA to 20 mA in steps of 2 mA.

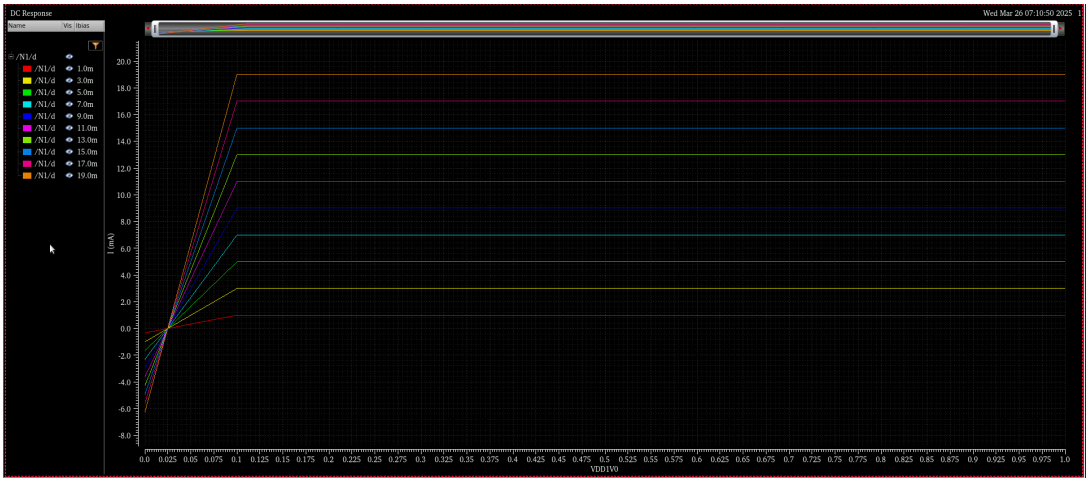


Figure 6.3: Drain Current vs. Drain Voltage Characteristic Curves

The following measurements are obtained by performing a DC Sweep on V_D, identical to the previous case. These results are shown in Figure 6.4. In Figure 6.5, the same measurement is presented with the drain current I_D plotted on a logarithmic scale.

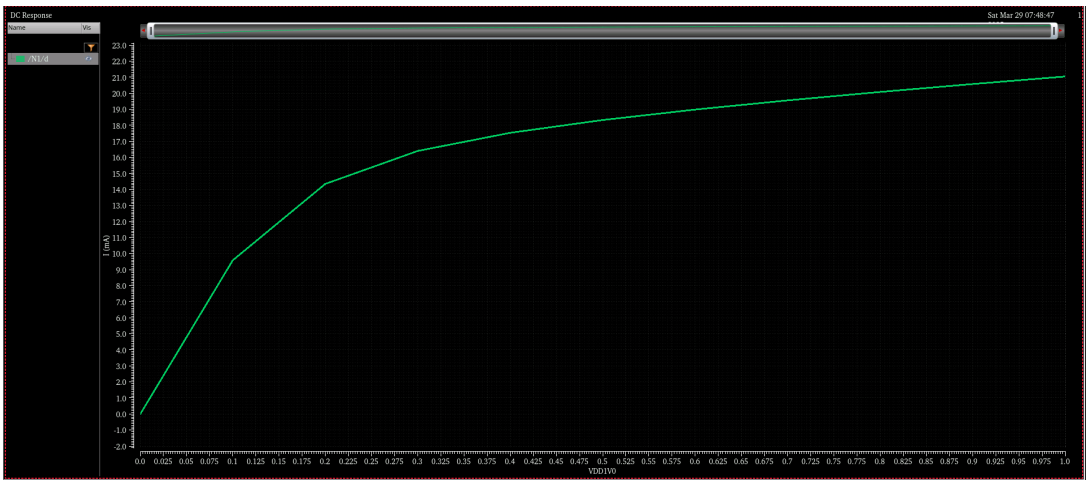


Figure 6.4: Drain Current vs. Drain Voltage

I_D vs. V_G

Next, the drain current is plotted both on a linear and a logarithmic scale as a function of the gate voltage V_G, as shown in Figure 6.6 and Figure 6.7, respectively.

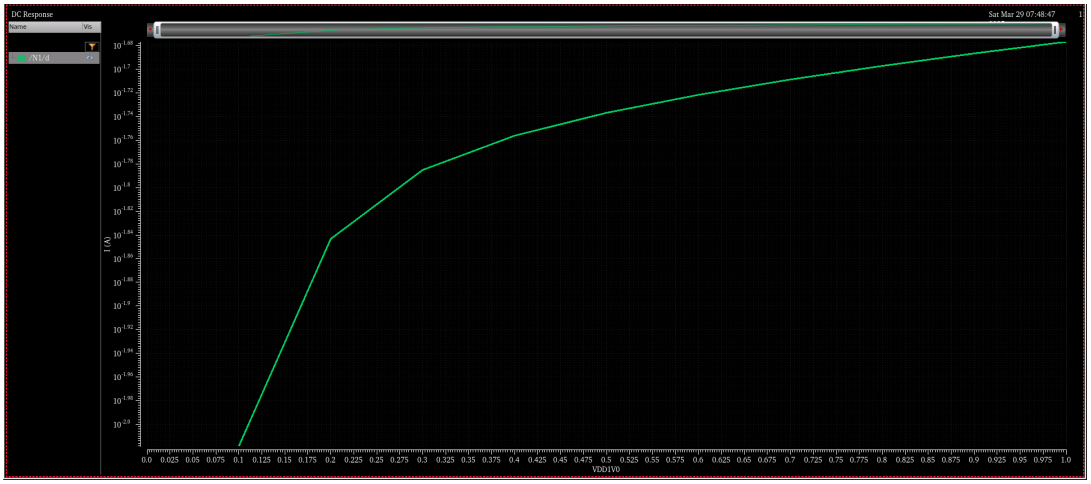


Figure 6.5: Drain Current vs. Drain Voltage (Logarithmic Scale)

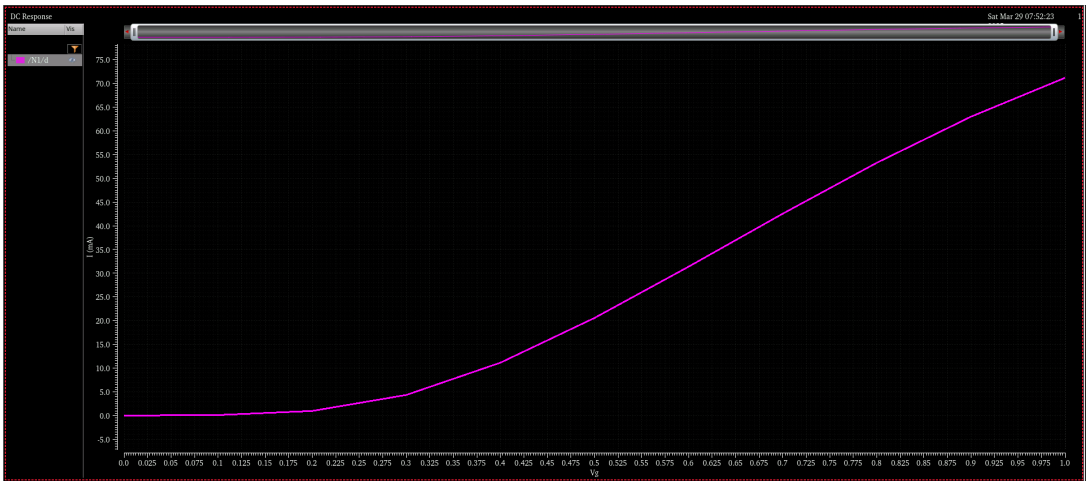


Figure 6.6: Drain Current vs. Gate Voltage

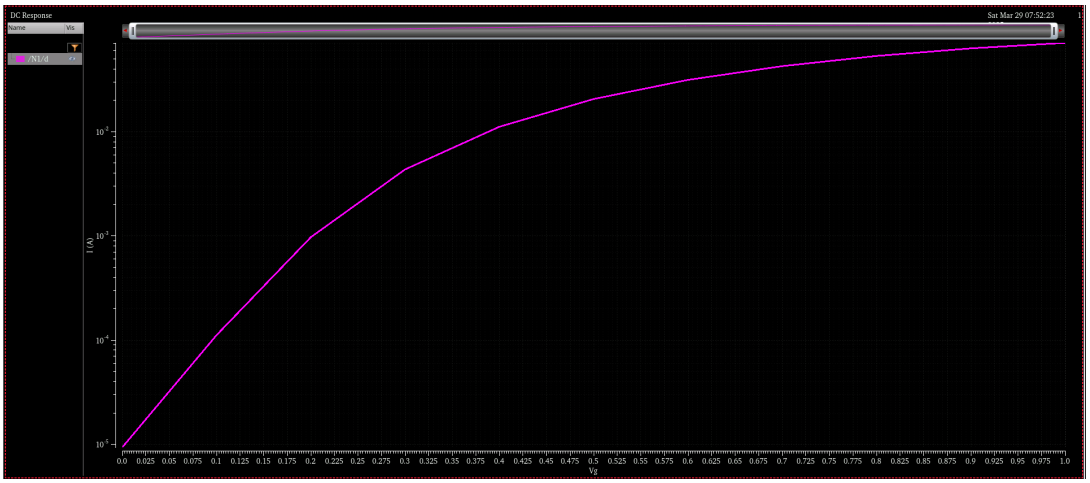


Figure 6.7: Drain Current vs. Gate Voltage (Logarithmic Scale)

Transconductance G_m

The most important small-signal parameter is the gate transconductance G_m. The corresponding characteristic curve is derived from the derivative of the drain current with respect to the gate

voltage,

$$G_m = \frac{dI_D}{dV_G}$$

as shown in Figure 6.8.

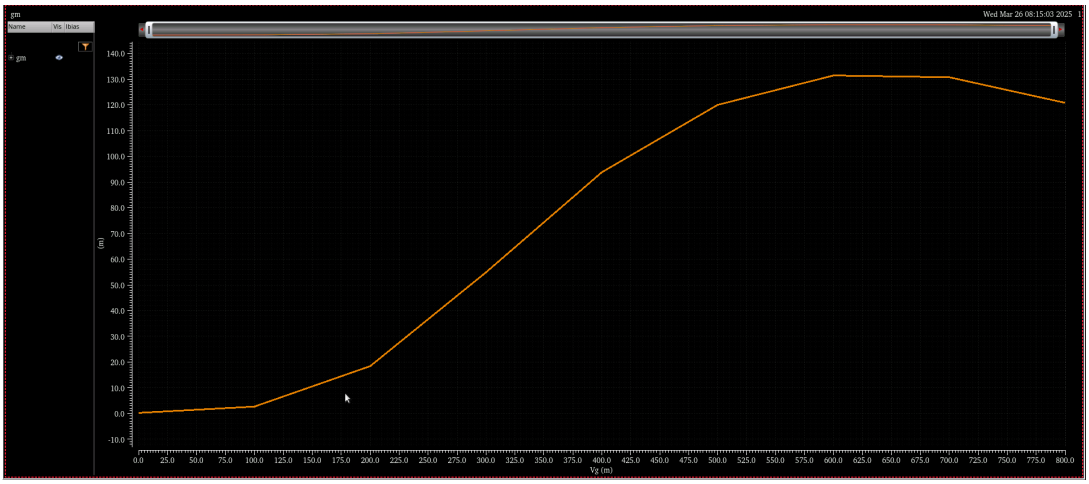


Figure 6.8: Transconductance G_m vs. Gate Voltage Curve

6.2.1 LNA Circuit Design Overview

The design steps followed for the development of the LNA using 22-FDX technology are based on a similar design methodology and approach as described in detail in Chapter 5, which concerns the design of an LNA using GaN HEMT technology. This approach is aligned with the methodology outlined in the article ”Algorithmic Design of CMOS LNAs and PAs for 60-GHz Radio.”

The selected topology, as in the previous case, is the cascode configuration (Chapter 5.2.2 – Core Design Strategy for LNAs). The combination of a common-source and a common-gate device enables the achievement of high overall gain, improved linearity, and reduced signal distortion. Additionally, this topology facilitates the matching of the LNA to the source impedance (typically 50 Ohms), which is crucial for maximizing power transfer and minimizing reflections.

The design process begins with an analysis of the key performance parameters of the LNA, such as Noise Figure, Gain, Linearity, and Stability. The objective is to complete the design while achieving minimum noise and maximum gain at the amplifier’s operating frequency.

Following a detailed description of the design steps, based on the methodology proposed in the aforementioned article, a comparative table is presented. This table juxtaposes the results of the implemented design with other related works found in the literature.

6.2.2 Step 1: Biasing for Minimum Noise Figure

The first step in the design process focuses on determining the optimal bias point that minimizes the noise figure of the transistor. This is achieved based on the current density. As stated in the referenced article, "Set the bias to the optimum NF_min current density (J_opt) to minimize the transistor noise figure. It is approximately 0.15 mA/μm, independent of the CMOS technology node or foundry."

To identify this optimal point, a DC sweep is performed on the device's multiplier parameter. The resulting plots, presented in Figure 6.9, illustrate the variation of NF_{min} as a function of the multiplier value (denoted as `mult`), which corresponds to the size scaling factor of the device. From the figure, it is observed that when `mult` = 32, the minimum noise figure NF_{min} is achieved. At this point, the drain current I_D is approximately 8 mA.

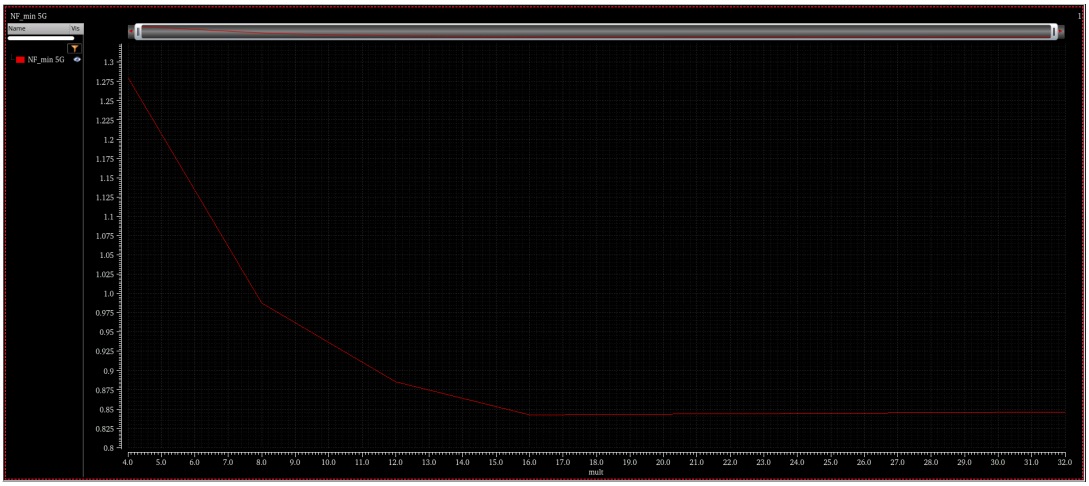


Figure 6.9: NF_{min} vs. Multiplier

6.2.3 Step 2: Optimal Finger Width to Minimize NF_{min}

The second step aims to determine the optimal finger width (W_f) in order to minimize the minimum noise figure (NF_{min}). According to the referenced article, for a 90 nm CMOS

technology, the optimal W_f is typically around 1–2 μm. Based on this guideline, a new sweep analysis was performed for W_f values ranging from 1 μm to 2 μm, and the corresponding noise performance of the device was evaluated.

As illustrated in Figures 6.10 and 6.11, it is evident that the lowest noise figure and simultaneously the highest maximum available gain (G_{max}) are achieved when $W_f = 1\,\mu$m. Therefore, this value was initially selected as the optimal finger width. However, during the input matching stage of the LNA design, the finger width was adjusted to 2 μm in order to improve the overall matching performance. Throughout both Step 1 and this step, the number of fingers (NoF) was kept constant at 8. As a result, the total gate width of the transistor is calculated as follows:

Total Gate Width = NoF × W_f × mult = 8 × 2 μm × 32 = 512 μm

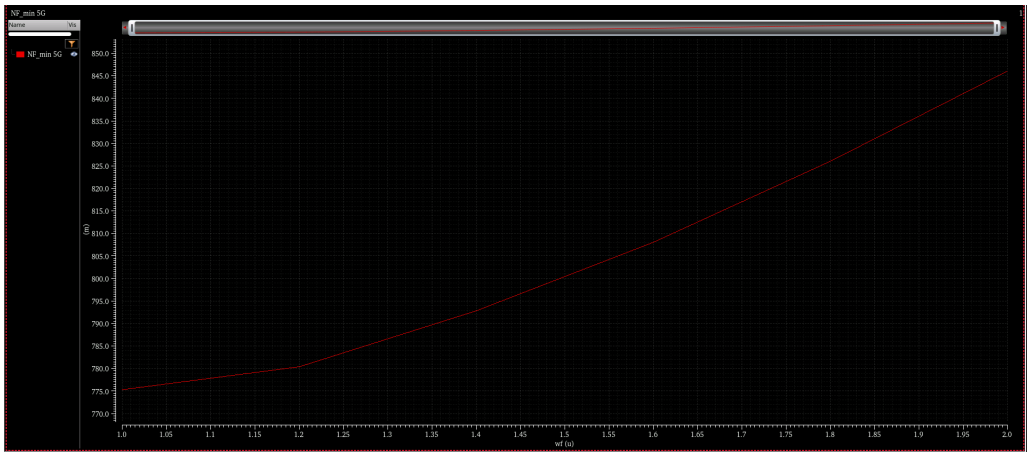


Figure 6.10: NF_{min} vs. Finger Width

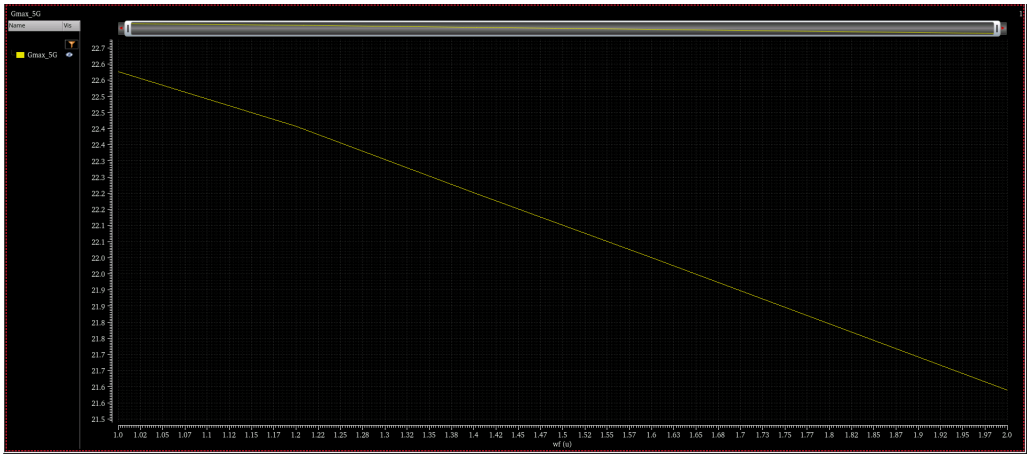


Figure 6.11: G_{max} vs. Finger Width

6.2.4 Step 3: Optimal Number of Fingers to Minimize NF_{min}

In this step, a new sweep is performed for the number of fingers (NoF), and using S-parameter analysis, the results and the behavior of the device are examined for three different NoF values (4, 6, 8). As shown in Figure 6.12, the minimum value of NF_{min} is achieved when the number of fingers is 6, while the highest value of G_{max} is obtained when the number of fingers is 4.

Based on the criterion of minimizing the noise figure, a NoF value of 6 would be considered optimal. However, in the following Step 4, it is found that for optimal input matching, the number of fingers needs to be set to 8. This choice does not significantly degrade either the noise figure or the gain of the device, and is therefore deemed the most appropriate.

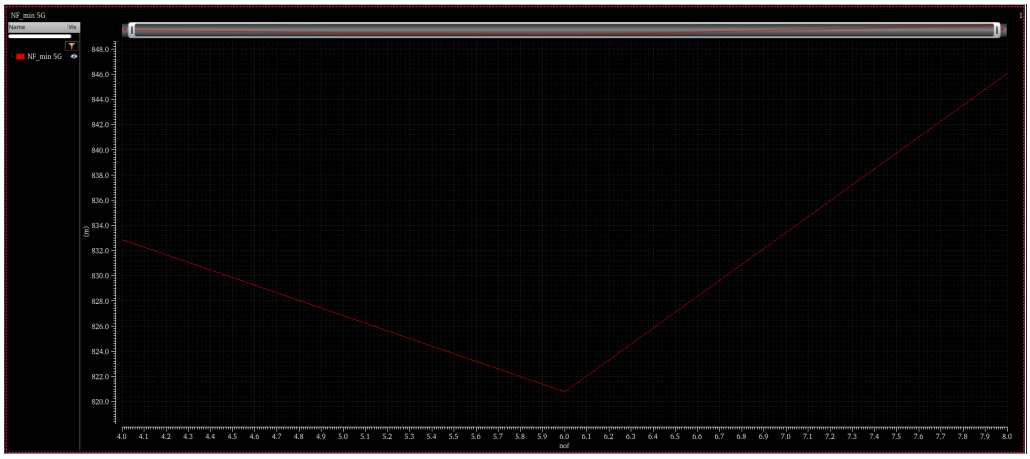


Figure 6.12: NF_{min} vs. Number of Fingers

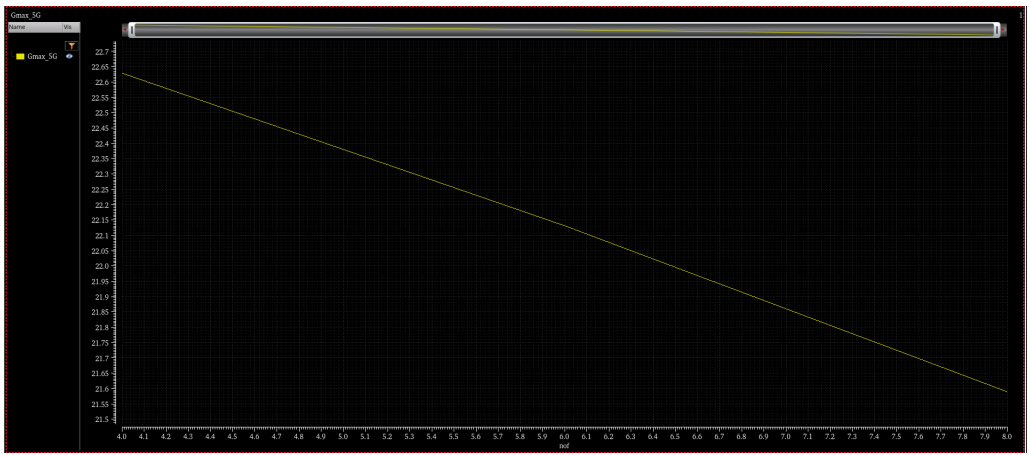


Figure 6.13: G_{max} vs. Number of Fingers

6.2.5 Step 4: Inductive Degeneration Technique

This step has been described in detail in Section 5.2.5, and the same methodology is applied in this technology for implementing input matching. According to the inductive degeneration technique, an inductor L_S is placed in series with the source terminal of the transistor. By selecting an appropriate value for L_S, the real part of the amplifier's input impedance can be adjusted to approximately 50 Ω. This ensures maximum power transfer from the antenna to the LNA while simultaneously minimizing signal reflections. Additionally, the presence of L_S contributes to a reduction in the overall noise and enhances the stability of the amplifier circuit.

Based on the small-signal model analysis of the transistor (as discussed in Section 5.2.5), the following equation can be used to determine an initial estimate for the inductor L_S:

$$Z_{\text{in}} = \frac{g_m L_S}{C_{gs}} + j\left[\omega(L_G + L_S) - \frac{1}{\omega C_{gs}}\right] \tag{6.1}$$

Subsequently, to determine the value that brings the real part of the input impedance as close as possible to 50 Ω, a parameter sweep is performed in the vicinity of the initial theoretical estimate. As a result, the value of the source inductor was selected to be $L_S = 350$ pH.

6.2.6 Step 5: Addition of L_G for Input Matching Tuning

The simplified expression for the input impedance Z_{in}, shown in Equation 6.1, necessitates the addition of an extra inductor L_G. This inductor is connected to the gate terminal of the transistor and is used to cancel the imaginary part of the input impedance. Using Equation 6.1 once again, an initial theoretical estimation for the value of L_G is obtained. A parameter sweep is then performed to identify the value of L_G for which the imaginary component of Z_{in} approaches zero. Following this procedure, the value of L_G was selected to be 2 nH.

This technique is particularly critical in the LNA design process, as it aims to perfect the input matching of the amplifier. In doing so, it ensures the optimization of the S_{11} parameter at the target operating frequency.

After identifying the optimal values for the inductors L_G and L_S, the resulting S_{11} plot is shown in Figure 6.14. From the plot, it is evident that the amplifier achieves excellent input matching at the desired frequency. The value of S_{11} falls below $-30\,\text{dB}$, indicating extremely low reflections and nearly ideal power transfer from the source to the amplifier.

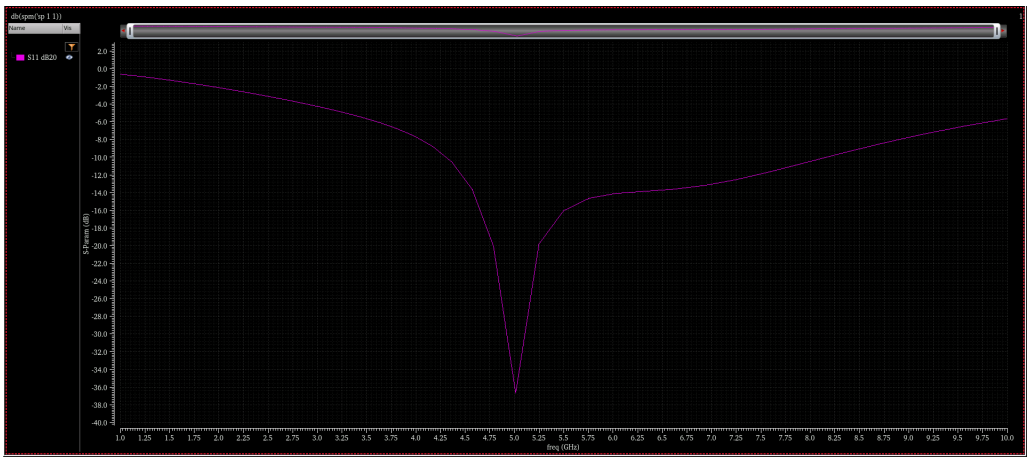


Figure 6.14: S_{11} after Input Matching

6.2.7 Step 6: Scaling the Size of the Cascode Device

At this stage, having already selected the optimal values for the inductors and having determined the appropriate sizing for the common-source device, the cascode device must now be added and properly dimensioned.

In this case, for the sake of symmetry and to simplify the amplifier design, the cascode device is chosen to be identical to the one used in the common-source stage, adopting the same number of fingers and the same finger width (W_f).

It is important to note that, in order to achieve maximum power transfer, the output impedance of the common-source device should be as close as possible to the input impedance of the cascode device. Moreover, the proper sizing of the cascode device is crucial not only for maintaining low noise but also for minimizing parasitic effects, particularly at high frequencies.

At this point, it should be noted that the cascode device is also biased using a DC voltage source, which is appropriately adjusted so that the voltage applied to the drain (V_{drain}) is approximately evenly distributed between the two devices. Furthermore, the current must remain stable even after the addition of the cascode device.

6.2.8 Step 7: Add Output Matching Network

The final step, as described in the reference article, is to add an output matching network with an inductive load in order to maximize gain. Specifically, an output matching network must be designed to match the output of the amplifier to the load (typically 50 Ω), thereby minimizing signal reflections and enabling maximum power transfer.

Figure 6.15 illustrates the output matching network implemented for the purposes of this design.

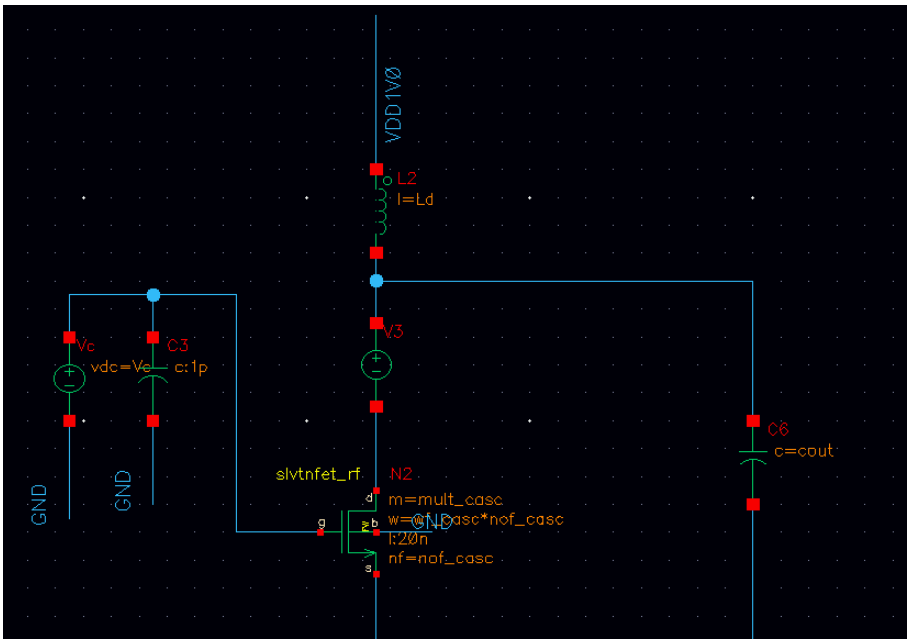


Figure 6.15: Output matching network.

The inductor L_D acts as the load at the output of the cascode device and contributes to the biasing of the amplifier. However, in combination with the output capacitor, it also facilitates the formation of a resonant circuit. The capacitor C_{out} plays a critical role in tuning the output to the operating frequency (5 GHz) and enables the transfer of maximum power to the load. Additionally, the capacitor functions as a DC-blocking element, preventing any DC component from reaching the load.

6.2.9 Design Validation and Results of the LNA

This section presents the final simulation results for the design of the Low Noise Amplifier (LNA), which has been optimized for operation at 5 GHz. The circuit's performance is evaluated based on key design specifications and critical parameters such as the noise figure, gain, input and output matching, linearity, and stability. The following results reflect the ideal case before layout (pre-layout), capturing the theoretical behavior of the circuit based on the initial design model.

Noise Figure (NF) and NF_{min}

Figure 6.16 presents the final values of the noise figure (NF) and the minimum achievable noise figure (NF_{min}). Achieving an NF value close to NF_{min} indicates effective input matching and proper overall biasing of the circuit. As shown, both NF and NF_{min} values are remarkably low, demonstrating that the amplifier introduces minimal additional noise to the signal.

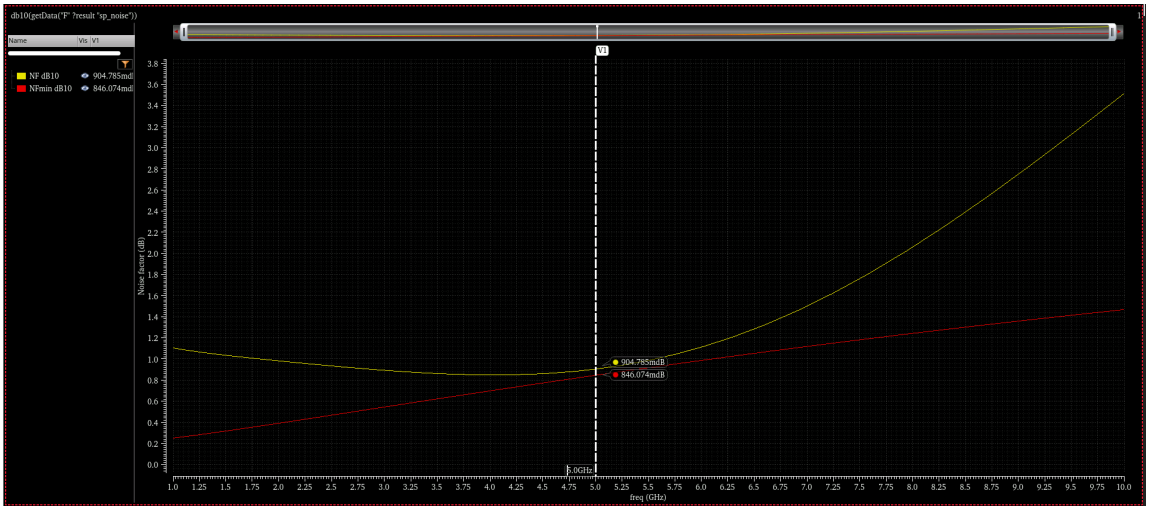


Figure 6.16: Noise Figure and minimum achievable noise figure (NF_{min}).

Maximum Gain

Figure 6.17 shows that the maximum available gain reaches a very satisfactory level. This confirms both the suitability of the chosen technology and the effectiveness of the design parameters. High gain is especially critical for amplifying weak RF signals in front-end applications.

S-parameters (S_{11} and S_{22})

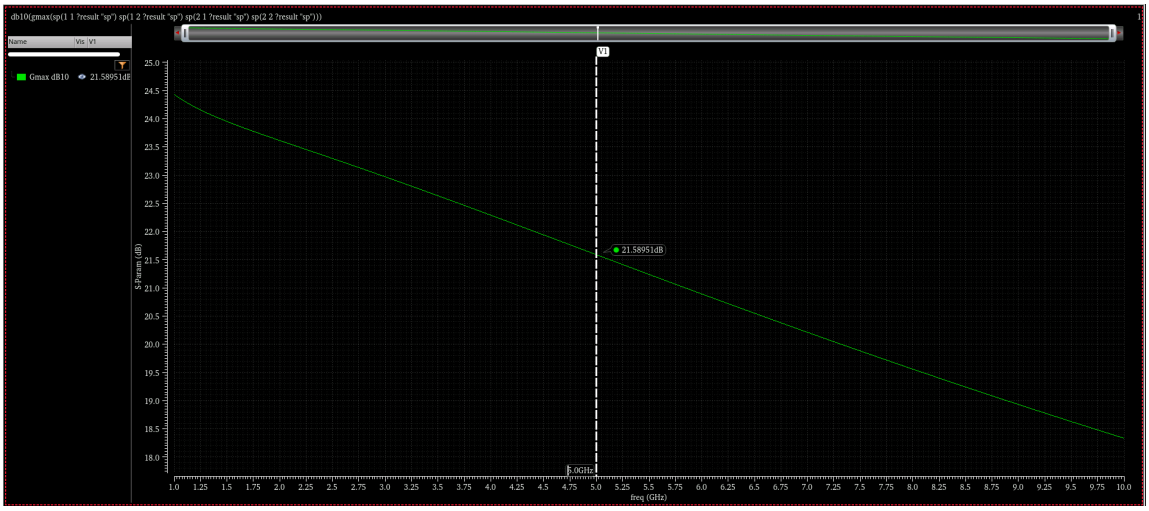


Figure 6.17: Maximum gain (G_{max}).

Figure 6.18 displays the S-parameters S_{11} and S_{22}, which are essential for assessing the power transfer efficiency and the stability of the circuit. Both parameters exhibit very low values (below ≈ -25 dB) at the operating frequency, indicating excellent input and output matching, respectively.

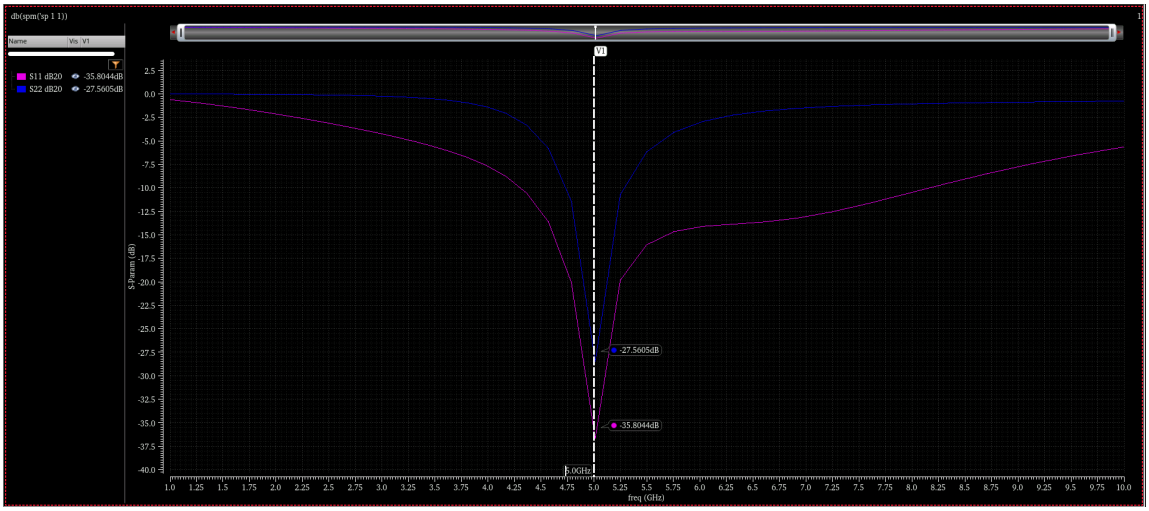


Figure 6.18: Input reflection coefficient S_{11} and output reflection coefficient S_{22}.

Stability Factors (K, Δ)

Figure 6.19 illustrates the stability factors K and Δ. As discussed in Chapter 3 (Section 3.1.6), a circuit is considered unconditionally stable if it satisfies the conditions $K > 1$ and $|\Delta| < 1$ across the entire frequency band. From the plot, it is evident that the proposed design meets these criteria, ensuring unconditional stability throughout the band of interest.

Input and Output Compression Points ($IIP3$, $OIP3$)

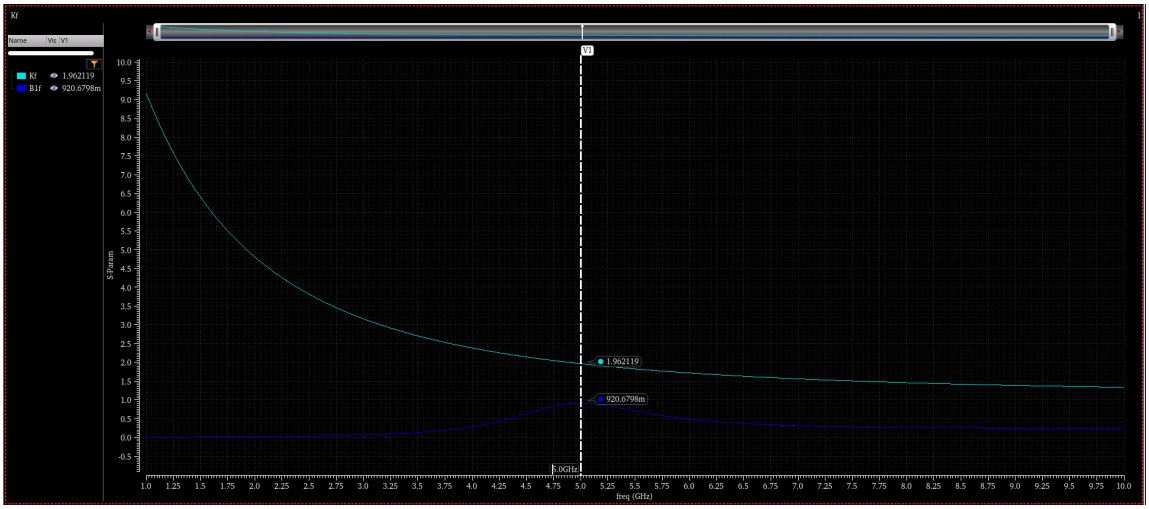


Figure 6.19: Stability factors K and Δ.

The linearity of the designed LNA is evaluated through the 1-dB compression point (P_{1dB}) and the third-order input intercept point ($IIP3$), two key parameters that characterize the amplifier's behavior under large signal conditions. As previously stated, the amplifier provides a gain of 21.56 dB, a value that is sufficient for low-noise applications. The 1-dB compression point is observed at $P_{\text{1dB}} = -3.27$ dBm, which is the input power level at which the actual gain drops by 1 dB due to transistor saturation. Additionally, the $IIP3$ is calculated to be -23.85 dBm.

The consistency of the simulation results is confirmed by the well-known theoretical relation:

$$P_{\text{1dB}} = IIP3 + \text{Gain}$$

which for the measured values gives:

$$P_{\text{1dB}} = -23.85 + 21.56 = -2.29 \text{ dBm}$$

This result closely approximates the simulated value of $P_{\text{1dB}} = -3.27$ dBm, thus validating the simulation and confirming the internal consistency of the model.

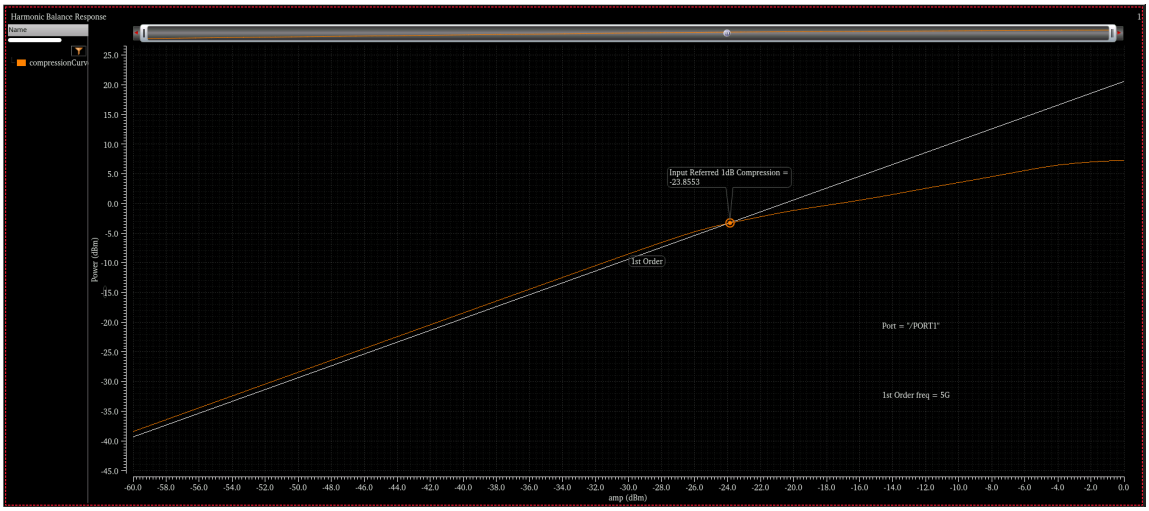


Figure 6.20: Input Compression Point

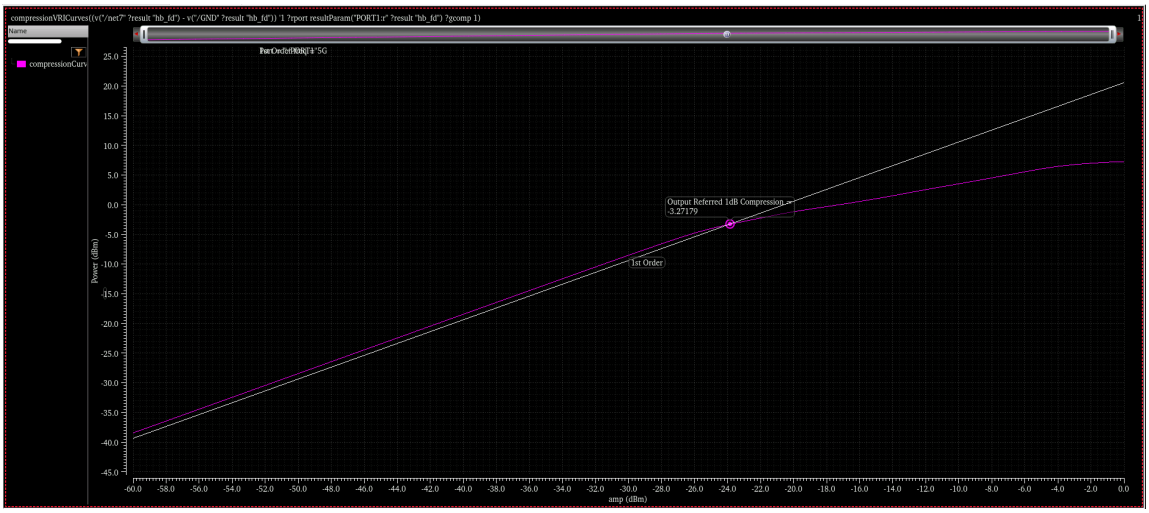


Figure 6.21: Output Compression Point

6.3 Evaluation and Comparison with Other Works

Table 6.3 presents a detailed comparison of the designed LNA with other recently published works. The performance metrics such as gain, noise figure (NF), input/output matching (S_{11}, S_{22}), and linearity parameters (P1dB and IP3) are evaluated across different CMOS technologies. The proposed LNA demonstrates a significant improvement in gain and noise figure while maintaining competitive input and output matching. Notably, it achieves the lowest S_{11} among all compared designs, indicating excellent input matching. This comparison highlights the effectiveness of the cascode CS-CG topology adopted in this work.

Initially, Table 6.2 presents the final design parameters and values that were determined for

the implementation of the proposed low-noise amplifier:

Table 6.2: Key Parameters of the LNA Transistor and Matching Network Elements

Desing Parameter	**Value**
1. V_{drain}	1.8 V
2. Gate Length (L)	20 nm
3. Finger Width (W)	2 μm
4. Number of Fingers (NoF)	8
5. Number of Multipliers	32
6. Gate (Series) Inductor L_{S}	2 nH
7. Source (Degeneration) Inductor L_{G}	350 pH
8. Drain Inductor L_{d}	3 nH
9. Output Capacitor C_{out}	190 fH

Table 6.3: Performance Comparison of the Proposed LNA with State-of-the-Art Designs

Comparison with Other Works							
Parameter	**[32]**	**[33]**	**[34]**	**[35]**	**[36]**	**[38]**	**This Work**
Process	0.18μm CMOS	0.18μm CMOS	22nm CMOS	0.18μm PDSOI	0.18μm CMOS	0.18μm CMOS	**22nm FDSOI**
Frequency (GHz)	5.4	3–5	5.5	5	5.4	5.2	**5**
Structure	CS–CS	Interstage Matching Inductor	Cascade with Inductive Degeneration	Cascode with Inductive Degeneration	CG–CS	CS Current Reuse	**Cascode CS–CG**
NF (dB)	0.423	4.5	0.73	1.9	2.4	2.94	**0.904**
Gain (dB)	12.54	12.7	20.5	9.3	19	13.6	**21.56**
P1dB (dBm)	NA	NA	NA	-7	NA	NA	**-3.27**
IP3 (dBm)	NA	3.1	NA	6.5	-2	NA	**-23.85**
S_{11} **(dB)**	-23.84	<-6	-19.9	-22	<-15	-16.6	**-35.8**
S_{22} **(dB)**	-17.47	<-5	NA	NA	<-10	-8.6	**-27.5**

Chapter 7

Conclusion and Future Work

The main objective of this thesis is the design of a Low-Noise Amplifier (LNA) that achieves low noise power while maintaining high performance. The work primarily focuses on presenting a detailed methodology for designing an LNA, which constitutes a critical component in the receiver chain.

This thesis explores two of the most important and modern technological platforms for RF circuit design: **Fully-Depleted Silicon-On-Insulator (FD-SOI)** and **Gallium Nitride High Electron Mobility Transistor (GaN-HEMT)**. FD-SOI technology, as an evolution of classical CMOS, achieves lower power consumption and reduced losses due to its thin insulating layer and fully isolated substrate. On the other hand, GaN-HEMT technology is an emerging and highly promising solution for high-power and high-frequency applications. A key element of this work is the parallel implementation of the same circuit topology (*Cascode Topology with Inductive Source Degeneration*) for both technologies at an operating frequency of 5 GHz. This approach enabled a direct comparison of the performance and characteristics of the two platforms, highlighting their advantages and limitations, and offering valuable insight for future RF design platform selection.

Several key figures of merit can be used for a comparative evaluation between the two technologies. These include the Noise Figure (NF) and two critical S-parameters: S_{21}, which reflects the amplifier gain, and S_{11}, which indicates the input matching quality. By observing the plots in Figures 7.1 and 7.2, it becomes evident that the GaN-HEMT technology achieves an unexpectedly low Noise Figure, approaching the theoretically minimum achievable value (NF_{min}). This suggests excellent performance in applications where noise minimization is critical.

However, in terms of gain performance, the S_{21} of the GaN-HEMT-based amplifier appears to be approximately 6.5 dB lower than that of the 22FDX technology. This does not necessarily

pose a problem, as gain requirements vary depending on the specific application and design objectives. As for the S_{11} parameter, both technologies demonstrate values lower than -35 dB, confirming excellent input matching of the amplifier.

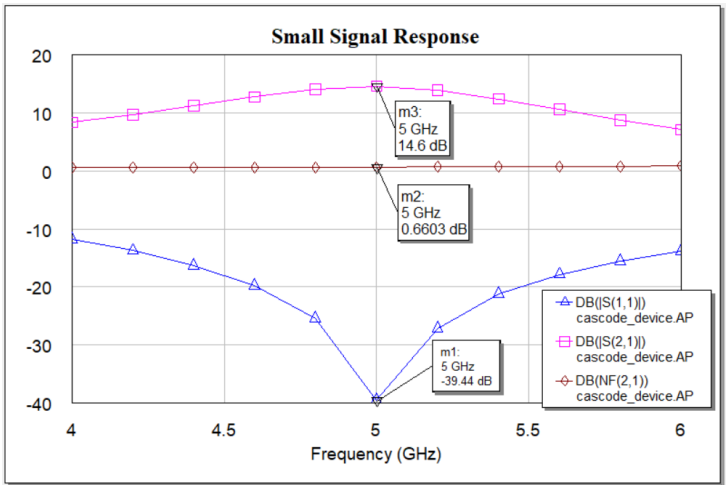


Figure 7.1: Small-signal response of the LNA using GaN-HEMT technology

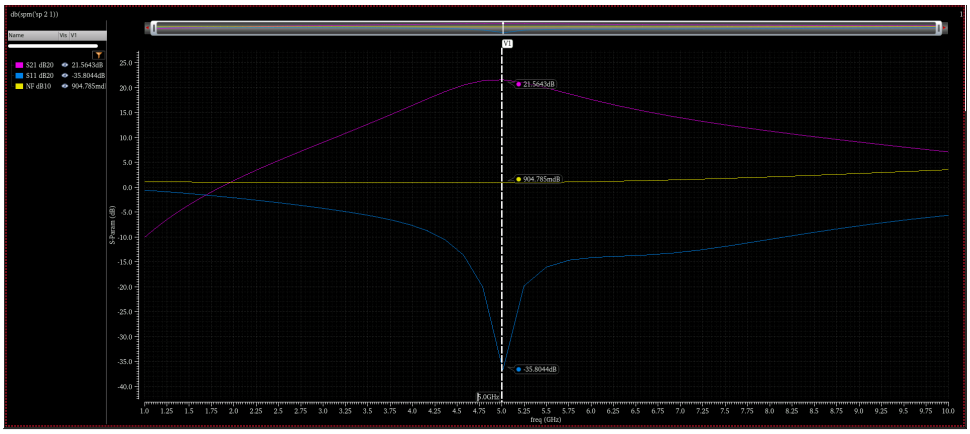


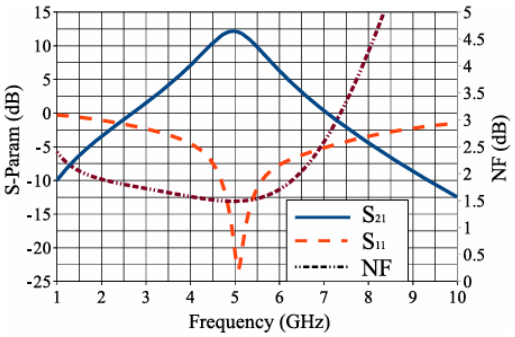
Figure 7.2: Small-signal response of the LNA using 22FDX technology

At this point, the paper *"Multi-objective Low-Noise Amplifier Optimization Using Analytical Model and Genetic Computation"*[16] proved particularly valuable for interpreting and validating the results of the present work. This paper provides a holistic approach to low-noise amplifier design by integrating genetic algorithms with analytical models, thereby combining theory with practical implementation.

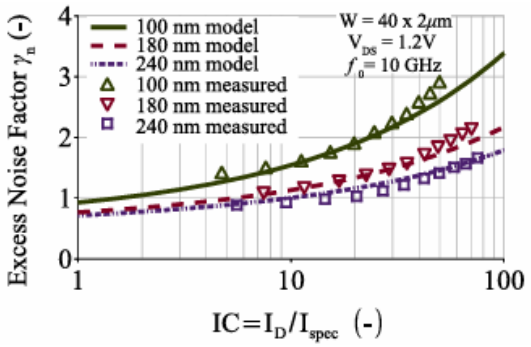
Specifically, the referenced paper focuses on the design of a common-source LNA with inductive degeneration, operating at 5 GHz and utilizing 90nm CMOS technology. The design takes into account the parasitic elements of the structure, making the results more

realistic. Although the architectural and technological implementation differs from this thesis, a comparison of the two reveals common optimization patterns and design trends—such as the concurrent achievement of low Noise Figure, sufficient gain (S_{21}), and improved impedance matching (S_{11}).

According to the design results shown in Figure 7.3a, the paper reports a high-performance LNA with a gain of $S_{21} = 13.2\,\text{dB}$, a low Noise Figure of $1.48\,\text{dB}$, and excellent input/output matching, with values of $S_{11} = -23.2\,\text{dB}$ and $S_{22} = -20.5\,\text{dB}$ at the center frequency. While these results are indeed impressive, the present study is expected to achieve similarly high—or potentially even improved—performance levels, particularly with respect to noise reduction. Specifically, by incorporating parasitic effects during the layout phase and applying optimization techniques tailored to each technology, the overall functional performance of the amplifier can be significantly enhanced.



(a) Small-signal response of the LNA using 90nm CMOS technology



(b) Excess Noise Factor (γ_n) vs. Inversion Coefficient (IC)

Figure 7.3: Comparison of performance characteristics for the 90nm CMOS LNA design[15, 16]

Figure 7.3b illustrates the simulation and measurement results from the referenced paper regarding the Excess Noise Factor (γ_n) as a function of the Inversion Coefficient (IC). It is observed that for 100nm CMOS technology, an IC of approximately 8 yields a Noise Factor of about $\gamma_n \approx 1.4$. This value lies at the upper boundary of the moderate inversion region, offering good performance at the expense of relatively high current consumption. However, with the use of more advanced FDSOI CMOS technology, improved performance is anticipated. The technology enables dynamic threshold control, allowing the transistor to operate at lower IC values while maintaining a low Noise Figure. At the same time, it provides an optimized balance between gain and power consumption.

In conclusion, this thesis demonstrates the feasibility of achieving satisfactory performance specifications in LNA design by leveraging FD-SOI and GaN-HEMT technologies while adhering strictly to a systematic design methodology. However, the design was carried out at the pre-layout level. As parasitic effects remain a constant challenge, it is deemed necessary to proceed with layout design and extraction in order to better evaluate the circuit behavior and obtain more realistic results. Moreover, Monte Carlo analysis provided by the *Cadence* tool proves particularly useful, allowing a statistical evaluation of the LNA's performance and variability under conditions of uncertainty and parameter variation. This involves running multiple simulations with randomly selected parameter values, effectively modeling external factors that influence circuit performance. A compelling direction for future work is the implementation of the designed LNA in a **differential architecture**. Transitioning from a single-ended to a differential output may result in improved linearity, stability, and overall amplifier performance, particularly in high-interference environments or in systems where signal integrity is critical.

Bibliography

[1] Texas Instruments, "Rf sampling for multi-band radios," Texas Instruments, Application Report SBAA328, Apr. 2019, accessed: 2025-07-19. [Online]. Available: https://www.ti.com/lit/pdf/sbaa328

[2] everythingRF. (n.d.) What is thermal noise? [Online]. Available: https://www.everythingrf.com/community/what-is-thermal-noise

[3] B. Bahreyni, *Fabrication and Design of Resonant Microdevices*, ser. Micro and Nano Technologies. William Andrew Applied Science Publishers, 2008. [Online]. Available: https://doi.org/10.1016/B978-081551577-7.50001-8

[4] S. Audio. (2025) Bandwidth calculating - cutoff frequencies calculator. [Online]. Available: https://sengpielaudio.com/calculator-cutoffFrequencies.htm

[5] A. S. Hindole, A. R. Jadhav, H. V. Dixit, and V. Gupta, "A cad based tutorial on microwave amplifier design," *International Journal of Engineering Research and Development*, vol. 4, no. 11, pp. 12–26, 2012.

[6] everything RF. (2020) What is ip3? everything RF. [Online]. Available: https://www.everythingrf.com/community/what-is-ip3

[7] F. P. Gozadinos, "Direct conversion receiver design for 2.7ghz lte band in tsmc90nm cmos," BroadCom, Tech. Rep., Jun. 2016, diploma Thesis, 81 pages, PDF version 1.7.

[8] B. Razavi, *RF Microelectronics*, ser. Communications Engineering and Emerging Technologies. Prentice Hall, 2012.

[9] N. Islam, M. F. P. Mohamed, M. F. A. J. Khan, S. Falina, H. Kawarada, and M. Syamsul, "Reliability, applications and challenges of gan hemt technology for

modern power devices: A review," *Crystals*, vol. 12, no. 11, 2022. [Online]. Available: https://www.mdpi.com/2073-4352/12/11/1581

[10] J. Kaushik, V. Balakrishnan, B. Panwar, and R. Muralidharan, "Analysis of fast and slow trap states on electrical performance of algan/gan hemts," in *2014 International Conference on Emerging Electronics (ICEE)*, Dec. 2014, pp. 1–4. [Online]. Available: https://doi.org/10.1109/ICEmElec.2014.7151145

[11] A. Zhaksylyk, "Implementation of a phase shifted full bridge dc-dc zvs converter with peak current mode control," Master's Thesis, Universidad de Oviedo, Aug. 2019. [Online]. Available: https://doi.org/10.13140/RG.2.2.33788.77445

[12] J. Zhao and W. Peng, "Lectures 6&7," 2006, lecture notes, 34 pages. [Online]. Available: https://mapl.cs.nycu.edu.tw/course/Electronics%2007/files/Lectures%206%267.pdf

[13] N. F. Tasirin, "Design of low noise amplifier (lna) in cmos process technology," Ph.D. dissertation, Universiti Teknologi Petronas, 2009.

[14] S. Semiconductor. (2023, June) Fd-soi: The disruptive innovation samsung foundry is leading to overcome the limits. Accessed: 2025-07-18. [Online]. Available: https://semiconductor.samsung.com/news-events/tech-blog/fd-soi-the-disruptive-innovation-samsung-foundry-is-leading-to-overcome-the-limits/

[15] A. Antonopoulos, M. Bucher, K. Papathanasiou, N. Mavredakis, N. Makris, R. K. Sharma, P. Sakalas, and M. Schroter, "Cmos small-signal and thermal noise compact modeling at high frequencies," *IEEE Transactions on Electron Devices*, vol. 60, no. 11, pp. 3726–3733, Nov. 2013. [Online]. Available: https://doi.org/10.1109/TED.2013.2283511

[16] A. Papadimitriou and M. Bucher, "Multi-objective low-noise amplifier optimization using analytical model and genetic computation," *Circuits, Systems, and Signal Processing*, vol. 36, 12 2017. [Online]. Available: https://doi.org/10.1007/s00034-017-0634-2

[17] T. Yao, M. Q. Gordon, K. K. W. Tang, K. H. K. Yau, M.-T. Yang, P. Schvan, and S. P. Voinigescu, "Algorithmic design of cmos lnas and pas for 60-ghz radio," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 5, pp. 1044–1057, 2007. [Online]. Available: https://doi.org/10.1109/JSSC.2007.894325

[18] K. Cheng and A. Khakifirooz, "Fully depleted soi (fdsoi) technology," *Science China Information Sciences*, vol. 59, no. 6, p. 061402, 2016. [Online]. Available: https://doi.org/10.1007/s11432-016-5561-5

[19] Y. Li, "Comparative analysis of working principles and applications of mosfet and hemt," *Applied and Computational Engineering*, vol. 65, pp. 66–74, 2024. [Online]. Available: https://doi.org/10.54254/2755-2721/65/20240470

[20] A. Hamdoun, "Design of GaN-based microwave components and application to novel high power reconfigurable antennas," Theses, Université de Rennes ; Carleton University, Oct. 2016. [Online]. Available: https://theses.hal.science/tel-01453383

[21] S. Chen, "Unlocking the potential of gallium nitride (gan) for third-generation semiconductors: Advantages, applications, and future prospects," *Highlights in Science, Engineering and Technology*, vol. 81, pp. 342–349, Jan. 2024. [Online]. Available: https://drpress.org/ojs/index.php/HSET/article/view/16243

[22] Z. Li, "Advancements in gan hemt structures and applications: A comprehensive overview," *Journal of Physics: Conference Series*, vol. 2786, no. 1, p. 012003, June 2024. [Online]. Available: https://dx.doi.org/10.1088/1742-6596/2786/1/012003

[23] A. M. Gamal, H. N. Ahmed, and M. A. El-Kfafy, "A quad-band 0.9/1.8/2.45/3.5 ghz, multi-standard, concurrent lna using a dual-band impedance transformer," in *2015 Asia-Pacific Microwave Conference (APMC)*, vol. 1, 2015, pp. 1–3. [Online]. Available: https://doi.org/10.1109/APMC.2015.7411598

[24] J. Shepard. (2022, Feb.) What is d-gan, e-gan and v-gan power? [Online]. Available: https://www.powerelectronictips.com/what-is-d-gan-e-gan-and-v-gan-power-faq/

[25] P. Xu, Y. Jiang, Y. Chen, Z. Ma, X. Wang, Z. Deng, Y. Li, H. Jia, W. Wang, and H. Chen, "Analyses of 2-deg characteristics in gan hemt with aln/gan super-lattice as barrier layer grown by mocvd," *Nanoscale Research Letters*, vol. 7, no. 1, p. 141, 2012. [Online]. Available: https://doi.org/10.1186/1556-276X-7-141

[26] M. Edwall, "Low-noise amplifier design and optimization," M.Sc. thesis, Luleå University of Technology, Luleå, Sweden, 2008, iSRN: LTU-EX-08/230-SE. [Online]. Available: https://www.diva-portal.org/smash/get/diva2:1032511/FULLTEXT01.pdf

[27] S. Zarrik, A. Bendali, F. ALtalqi, K. Benkhadda, S. Habibi, Z. Sahel, M. El Kobbi, A. Hadjoudja, and M. Habibi, "Designing common-source low noise amplifier utilizing gan hemt for sub-6 ghz in 5g wireless applications," *TELKOMNIKA (Telecommunication Computing Electronics and Control)*, vol. 23, no. 1, pp. 48–56, 2024. [Online]. Available: https://journal.uad.ac.id/index.php/TELKOMNIKA/article/view/26324

[28] C. Andrei, O. Bengtsson, R. Doerner, S. A. Chevtchenko, and M. Rudolph, "Robust stacked gan-based low-noise amplifier mmic for receiver applications," in *2015 IEEE MTT-S International Microwave Symposium*, 2015, pp. 1–4. [Online]. Available: https://doi.org/10.1109/MWSYM.2015.7166766

[29] O. M. Abbas and A. Jarndal, "On the design of gan low noise amplifier for 5g applications," in *2022 International Conference on Electrical and Computing Technologies and Applications (ICECTA)*, 2022, pp. 178–181. [Online]. Available: https://doi.org/10.1109/ICECTA57148.2022.9990078

[30] M.-S. Kim and S.-S. Yoo, "Rf-soi low-noise amplifier using rc feedback and series inductive-peaking techniques for 5g new radio application," *Sensors*, vol. 23, no. 13, 2023. [Online]. Available: https://www.mdpi.com/1424-8220/23/13/5808

[31] T. Peng, J. Liu, and W. Wang, "A low power 2.5–5 ghz low-noise amplifier using 0.5-µm gaas phemt technology," *Journal of Semiconductors*, vol. 33, no. 10, p. 105001, oct 2012. [Online]. Available: https://doi.org/10.1088/1674-4926/33/10/105001

[32] S. U. Shankar and M. D. K. Dhas, "Design and performance measure of 5.4 ghz cmos low noise amplifier using current reuse technique in 0.18 μm technology," *Procedia Computer Science*, vol. 47, pp. 135–143, 2015. [Online]. Available: https://doi.org/10.1016/j.procs.2015.03.192

[33] S.-K. Wong, F. K. W. Lee, S. Maisurah, M. N. B. Osman, and S. J. Hui, "Design of 3 to 5 ghz cmos low noise amplifier for ultra-wideband (uwb) system," *Progress In Electromagnetics Research C*, vol. 9, pp. 25–34, 2009. [Online]. Available: https://doi.org/10.2528/PIERC09062202

[34] H. Singh, "Low noise amplifier for 5ghz wi-fi applications on 22nm," 2024, retrieved from University of Arkansas ScholarWorks. [Online]. Available: https://scholarworks.uark.edu/eleguht/91

[35] A. Madan, M. J. McPartlin, C. Masse, W. Vaillancourt, and J. D. Cressler, "A 5 ghz 0.95 db nf highly linear cascode floating-body lna in 180 nm soi cmos technology," *IEEE Microwave and Wireless Components Letters*, vol. 22, no. 4, pp. 200–202, 2012. [Online]. Available: https://doi.org/10.1109/LMWC.2012.2187882

[36] D. Gangopadhyay, S. Shekhar, J. Walling, and D. Allstot, "A 1.6 mw 5.4 ghz transformer-feedback gm-boosted current-reuse lna in 0.18 µm cmos," in *ISCAS 2010 - 2010 IEEE International Symposium on Circuits and Systems: Nano-Bio Circuit Fabrics and Systems*, Jul. 2010, pp. 1635–1638. [Online]. Available: https://doi.org/10.1109/ISCAS.2010.5537466

[37] T. O. Dickson, K. H. K. Yau, T. Chalvatzis, A. M. Mangan, E. Laskin, R. Beerkens, P. Westergaard, M. Tazlauanu, M.-T. Yang, and S. P. Voinigescu, "The invariance of characteristic current densities in nanoscale mosfets and its impact on algorithmic design methodologies and design porting of si(ge) (bi)cmos high-speed building blocks," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 8, pp. 1830–1845, 2006. [Online]. Available: https://doi.org/10.1109/JSSC.2006.875301

[38] P.-T. Sun, S.-S. Liao, H.-L. Lin, C.-F. Yang, and T.-W. Yang, "The design of low noise amplifier with gain-controlled and low power consumption for wlan applications," in *PIERS Proceedings*, Beijing, China, Mar. 2009, pp. 906–910, presented at Progress in Electromagnetics Research Symposium (PIERS), March 23–27, 2009. [Online]. Available: https://www.researchgate.net/publication/283739286_The_design_of_low_noise_amplifier_with_gain-controlled_and_low_power_consumption_for_WLAN_applications