Control and communication for smart photovoltaic arrays

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ABSTRACT

Decarbonization of energy generation is required to address the urgent need to combat climate change and meet the Paris Agreement targets. Photovoltaic Systems (PVS) are a major contributor to this solution, and they are expected to grow significantly faster than any other renewable-energy technology in the coming years due to their appealing features. This paper discusses the development of a two-way communication protocol between two transceivers and a custom-designed communication board installed on each PV array. With this configuration, it is possible to transmit the measurements of each PV cell in the array to a data recording and monitoring service. Additionally, the application can customize the operation of the strings that make up the array, by broadcasting special commands to them. A prototype experimental setup was constructed in order to test the communication between the PV array communication board and the uplink/downlink transceivers. The experimental results verify the feasibility and effectiveness of the proposed communication protocol between the Electronics Interface System (EIS) and the Smart PV array since the communication protocol meets the specification for transmitting the information from 1000 smart PV cells within one minute, as well as the strict timing requirements by the protocol for transmitting the parameters to the PV strings.

CCS CONCEPTS

• **Hardware** → Printed circuit boards; PCB design and layout; Communication hardware, interfaces and storage; Power and energy; Integrated circuits.

KEYWORDS

Power line communication, Communication protocols, PCB Design, Smart Grid, Photovoltaics

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1 INTRODUCTION

The use of photovoltaic (PV) systems in power generation is becoming increasingly popular [1]. According to Eurostat, solar power is the fastest-growing source: from 2008 to 2020, the amount of electricity generated by solar power increased from 7.4 TWh in 2008 to 144.2 TWh in 2020, meaning an increase of approximately 1848% [2].

PV systems (PVS) power generation is easily integrated into the automotive industry, and more specifically into electric car charging stations [3]. In addition, PVS are being applied to public transport [4, 5], but their application has also recently started as an auxiliary energy source in unmanned aircraft [6, 7]. On the other hand, the low-profit margin of a PV installation [8], in connection with the still low efficiency of the PV cells used in PV installations [9, 10], are significant problems for such an investment.

In conventional PVS, energy management is performed either in PV arrays or in individual groups of solar cells, resulting in a significant reduction in energy production. A smart PVS is composed of Smart Solar Cells, each of which consists of a conventional solar cell connected to a custom-designed Integrated Circuit (IC). Such an installation will aid in the maximization and management of the energy produced by each solar cell, as well as detection and isolation of faulty PV cells, ensuring maximum energy production [11, 12].

Directly connecting the Smart PV cells to the Electronics Interface System (EIS) via wiring is impossible, as this would increase the number of connectors required to such an extent that the overall PVS circuitry would be impossible to implement. For this reason, Power Line Communication (PLC) technology will be used [13]. PLC implementations found in the literature can be divided into two categories: those that can send data over an AC bus and those that can send data over a DC bus.

i. AC power implementations: The works of [14, 15] investigate linking the outputs of power converters in series, such as H-bridges and AC-stacked inverters.

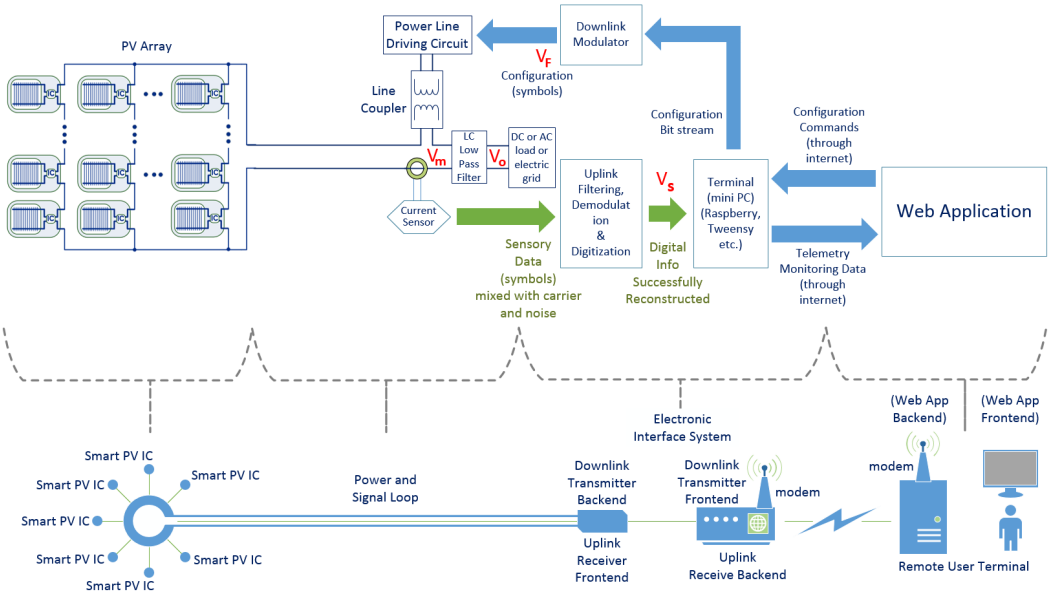

Figure 1: Smart PV array electronic diagram.

ii. DC power implementations: In order to produce the corresponding information-driven excitation, the works of [16] and [17] employ a coupling circuit paired in series or parallel with the power-producing module. The disadvantage of this architecture is that the modulation circuitry increases total power complexity and cost. An improvement to the above problem is to use two DC buses, one for input and one for output [18]. In [19], a commercial PLC transceiver was utilized to execute PLC communication on a DC bus containing series-connected PV cells. The circuit encodes information data as current pulses, eliminating the need for a shared reference voltage.

The PLC in [20], is hybrid and can send data to both AC and DC buses.

The purpose of this research is to present and examine a novel two-way communication protocol that was created for communication between the EIS and a Smart PV array. In the following sections of this paper, the operation of a smart PV array will be briefly presented and the operation and communication to and from the electronic interface system and the smart PV array will be analytically presented. The presentation of the experimental procedure will follow and the paper will close with the discussion and conclusions of its results.

2 SMART PV SYSTEM DESCRIPTION

The designed data transmission protocol is a two-way communication protocol based on the following subsystems:

i. The uplink interface receives the information sent from each cell of the Smart PV array and transmits the data to the user interface electronic system so that it can be sent to a monitoring web application.

ii. The downlink interface transmits the configuration on each string that composes the Smart PV array from the monitoring web application via the EIS that is attached to the Smart PV array.

Figure 1 shows the general diagram of the overall power transmission and communication system and the network schematic diagram of a Smart PV array. From left to right, the array of smart PV cells and the power transmission line are connected to the electrical load and/or the electrical grid. The power line transfers power and PV telemetry data by developing a voltage V_m at its output terminal. Once filtered, the power signal of the voltage V_o is connected to the load and/or the power grid. The power component of the V_m is removed by proper high-pass filtering and the high-frequency data signal is then digitally reconstructed as V_s (through the demodulation and digitization on the Uplink Receiver Frontend) device. The digital signal V_s is then further processed by the Uplink Receiver Backend and sent to the remote Web application.

The user can then monitor the meta-processed data and, if required, she/he can use the Web Application interface to update the PV array power configuration by sending special commands. These commands are directed to the Downlink Transmitter Frontend which forwards them, after proper processing, to the Downlink Transmitter Backend which, in turn, broadcasts the commanding bitstream as a series of symbols of voltage V_f to the Power Line Driving Circuit (PLDC). Finally, the PLDC injects the proper voltage waveforms to the common power bus, to be intercepted by the respective Smart PVs.

Figure 1 takes special care to depict the main subsystems of the terminal node (backend and frontend) presenting how the system involves the remote user to the system through the internet and how it mediates so that the user can monitor and configure the PV Array. Each Smart PV array consists of up to a thousand PV cells, divided into up to four PV strings.

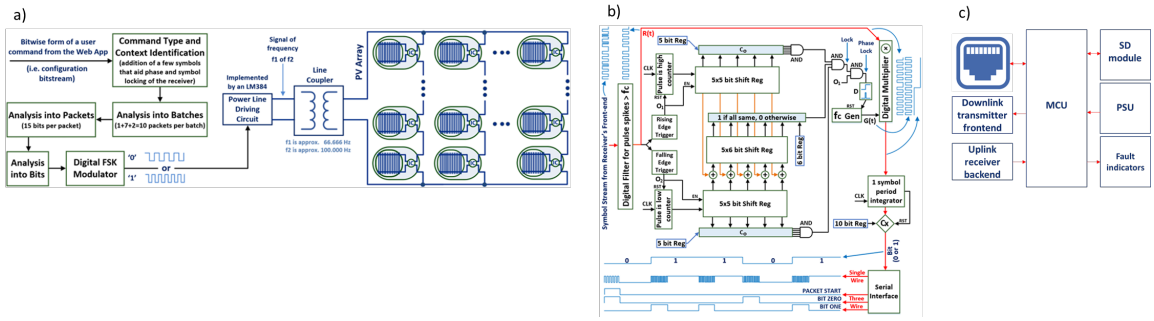

Figure 2: Interface modules [20].

2.1 Electronic interface system description

The EIS installed in each PV array consists of:

- A custom-designed PCB that contains an NXP iMXRT1062 microcontroller unit (MCU), that processes the data received from the PV cells through the Uplink Receiver Frontend and transmits them to the Web application service and vice versa (through the Downlink Transmitter Backend). The custom-designed communication board is presented in Figure 2c. Its firmware implements the Uplink Receiver Backend and the Downlink Transmitter Frontend. An ethernet network interface exchanges data with a web application via an MQTT server, as discussed in [11]. The custom-designed PCB connects to the Uplink Receiver Frontend and Downlink Transmitter Backend via a ribbon connector.
- A field-programmable gate array (FPGA) development board containing the Uplink Receiver Frontend (Figure 2b).
- An FPGA development board containing the Downlink Transmitter Backend (Figure 2a).

The EIS is connected to the power line of the PV array using special circuitry. All transmissions to and from the PV cells are performed via the main power line.

Each PV cell is connected to a custom-made IC that transmits its unique cell ID, operating voltage, and current measurements [21]. Furthermore, each cell receives its configuration through the EIS [22]. It should be noted that the cells belonging to the same string must be configured with the same settings.

Figure 2a presents the Downlink Transmitter Backend, which is comprised of two main parts, one digital and one analog. The digital one is developed as VHDL logic on an Intel DK-DEV-10M50A MAX10 FPGA development board. The block diagram that describes the operation of both the digital and the analog part is shown in Figure 2a. As it is vital to ensure that the PV Array will apply the received commands only if they are guaranteed to be correct, apart from the CRC concept, a multi-layer encryption technique has been adopted based on maximum length sequences or m-sequences. This is why the transmitter first analyses the command type and context of the commands it receives from the Downlink Transmitter Frontend. Each command carries 30 bits of sensitive information and 21 bits of CRC. These bits (or batches) are called high-level bits to distinguish them from the low-level bits, which are the actual transmission symbols, i.e., the symbol stream generated by the transmitter's output. The transmitter, apart from this stream of symbols that carry the information of the 51 high-level bits, also forms a header of a few special square waves with a format that can aid the receivers of the smart PVs to properly lock the phase and symbols of the transmitted signal to follow. The high-level bits (batches) comprise 1+7+2 packets (or medium-level bits). The 1st medium-level bit is called a header which also helps a packet locking mechanism on the receiver side. The next 7 bits hold the actual information (of 1 high-level bit) as an m-sequence, which can be identified as a '0' or a '1' depending on whether the 7-bit m-sequence is placed as is or logically inverted, and the last 2 medium level bits are the footer that helps proper packet locking.

Similarly, each packet is comprised of 15 low-level bits placed in a special 15-bit m-sequence, defining the logic state of the medium-level bits (packets) as '0' or '1' depending on the 15-bit m-sequence is placed as is or logically inverted. Finally, the analysis of the low-level bits means that there will be 10*15=150 low-level bits or symbols for each high-level bit. These symbols will either be a square wave of 4 periods at 66.6 kHz or a square wave of 6 periods at 100.0 kHz (holding in both cases the same amount of time, 60 μs). This means that every high-level bit requires 150*60 μs = 9 ms to be transmitted. The transmitter sends a high-level bit every 60 ms, which means there is a 60-9 = 51 ms time available for the transmission of the smart PVs (one at a time) to the EIS. This also means that a proper transmission of a whole command will take 51 * 60 = 3.06 s to be completed. If the designer suspects a high noise level, then the transmitter can be set to repeat every one of the high-level bits N times in order to increase robustness.

Figure 2b presents the Uplink Receiver Frontend, which comprises two main parts: analog and digital. The analog one is responsible for processing (in 3 main stages) the current sensor signal (shown in Figure 1). The first stage comprises a differential amplifier for proper signal sensing, the second stage includes a differential (high-pass) passive filtering, and the third stage has a level shifting and digitization circuitry (by a Schmitt-trigger comparator). Then the signal is forwarded to the second part of the Uplink Receiver Frontend device, which is developed as VHDL logic on an Intel DK-DEV-10M50A MAX10 FPGA development board.

The block diagram that describes its operation is shown in Figure 2b. Primarily, a digital filter is used to remove any remaining spikes. The cleaned $R(t)$ signal is then passed through a set of shift registers and comparators (C_o) which keep the CLK counts of each high and

Figure 3: FSM for the Downlink interface and four-wire interface example.

low pulse respectively, and compare the successive (sensed) periods to properly lock on the phase of the square waveform and to detect (lock) each symbol of the BPSK modulation. This design allows the detection of any pattern similar to the anticipated square wave of frequency f_c, thus suggesting the presence of the anticipated carrier signal and the proper locking of its phase and symbols.

Once the certainty of proper signal reception is achieved, the output signal $G(t)$ of the internal generator, which creates a square wave signal of similar frequency to the one received, is multiplied by the received signal $R(t)$ using a digital multiplier. This results in the down-conversion of the $R(t)$. By properly integrating the product of the digital multiplier per CLK and comparing it to a preset value (which is half of the CLKs that each symbol lasts) the down-converted signal is transformed to a discrete binary value, either 0 or 1. Finally, these values are transmitted through a serial interface that provides two asynchronous serial protocols (single-wire and three-wire) to the interface of the Uplink Receiver Backend device.

Each EIS has the same generic firmware, which is in charge of the initialization of the various subsystems and failure checks. Each EIS has a distinct configuration that is required to distinguish the Smart PV array and avoid conflicts with the neighboring arrays during their initialization. This unique configuration is provided via a configuration file. The configuration file contains the PV-park and PV-array unique-ID codes, as well as the necessary settings (IP address, gateway, subnet mask, DNS address, time configurations for downlink transmission) for each EIS. In addition, any event that occurs while the user interface is in use, is recorded in a log file. When the initialization is complete, the EIS receives the configurations for each of the smart PV Strings that compose the PV array, allowing the cells to begin transmitting their measurements.

The interface then packages the measurements received from each PV cell, with the identities of the solar park and PV array that correspond to the interface, along with a timestamp, and transmits the package to the monitoring web application for further processing.

2.2 Data transmission to the Smart PV cells

In order to configure each string of the Smart PV array and before sending the settings to the string (Functional Command), two additional commands are sent:

- The 1K-WakeUp command, in order for all the smart PV elements to be activated.
- The SYNC command, in order for the cells to coordinate and start transmitting information, without data collisions, according to the instructions of the following functional command that follows.

Commands must be sent according to specific timing and for this, a timer from the MCU is set from the configuration file of the EIS in order to control the state machine responsible to transmit data from the Downlink Transmitter Backend to the Downlink Transmitter Frontend and generate the necessary time delays according to the specified timing. The State machine that controls the configuration for the four strings that compose the Smart PV array is summarized in Figure 3a.

Concerning the communication of the MCU of the EIS (Downlink Transmitter Frontend) with the Downlink Transmitter Backend (FPGA), a four-wire interface was developed (similar to the three-wire one shown in paragraph 2.1) in which a wire is required as a bit to indicate the beginning of the packet. From the following pulse, the command or settings bits are transferred through the other 2 wires. One wire is used to send a pulse when the bit is “1” and the other wire is used when the bit is “0” (Figure 3b). The fourth wire is used to signify the end of the command. The period of each pulse corresponds to a time specified in the EIS configuration file. Each pulse has a 50% duty cycle. The default values for sending the commands from the Downlink transmitter backend to the Downlink transmitter frontend, through the FSM are state cycle: 1.5 ms, Wake-up command delay: 144 s, Sync command delay: 58.8 s, Functional command delay: 116.4s. All three commands are 51 bits in size, but the total information sent is 53 bits (2 extra start/stop bits). The first two commands (1K-WAKEUP, SYNC) always have a fixed value, which does not correspond to any parameter. Functional commands also consist of 51 bits with two extra start/stop bits. According to Figure 4, the 21 least significant bits of a functional command (positions 20-0) correspond to the CRC Checksum, while the 6 most

Bit No.	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34
Desc. (0/1)	DC/AC	50/60Hz	SA/GC	ON/OFF	STRb0	STRb1	0	1	0	1	Voltage Setting						
Bit No.	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17
Desc.	Voltage Setting			Power Setting										CRC Checksum			
Bit No.	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Desc.	CRC Checksum																

Figure 4: Functional Command bit analysis.

Bit No.	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34
Desc.	strID			clD							Voltage value						
Bit No.	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17
Desc.	Voltage value			Current value										CRC Checksum			
Bit No.	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Desc.	CRC Checksum																

Figure 6: Structure from the telemetry data transmitted via the Uplink interface.

significant bits (positions 50-45) correspond to the settings and the identifier of the string mentioned. The next 4 bits (positions 44-41), always have the value "0101" and are necessary for internal use in the back-end part of the downlink transmitter. The 20 intermediate bits correspond to the output voltage of the PV element (10 bits – positions 40-31) and the power value of the PV element (10 bits – positions 30-21).

2.3 Data transmission from the Smart PV cells

Regarding the communication of the EIS (Uplink receiver backend) with the Uplink receiver frontend (FPGA), a three-wire interface was developed, as shown in 2.1 (Figure 5). The time required to send the 51bits is listed in terms of the 60ms time slot corresponding to each PV cell.

According to this communication protocol, the Uplink receiver frontend uses one wire to transmit a pulse as a synchronization bit when starting to send the packet in parallel with the first information bit. The other 2 wires send a pulse when the information is "1" and "0", respectively. The period of each signal corresponds to 550 ms with a 50% duty cycle. The data sent is 51 bits in size. According to Figure 6, the 21 least significant bits correspond to the CRC Checksum (positions 20-0), while the 10 most significant bits (positions 50-41) correspond to the identifier of the PV string (positions 50-49) and in the identifier of the smart PV element (positions 48-41). The 20 intermediate bits correspond to the PV voltage (10 bits – positions 40-31) and the current value of the PV element (10 bits – positions 30-21). Sending the data of each PV cell to the EIS takes 28.05 ms (much less than the 51 available), within the 60 ms time slot allocated to it, in order to satisfy the specification that states that 1000 cells will send their data within one minute.

It should be noted that the time duration of the synchronization pulse for both sending and receiving data from the downlink and the uplink corresponds to a single half-period (parametric for the downlink interface and 275μs for the uplink interface). The communication on both the four-wire interface and the three-wire interface is implemented as active high. The connection between

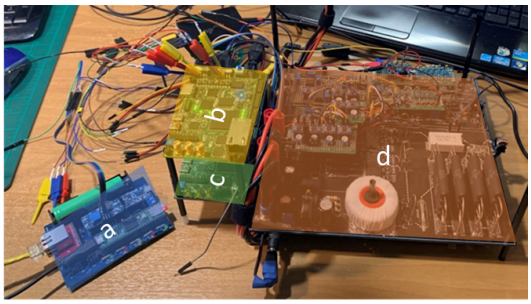

Figure 7: Experimental setup.

the Uplink receiver and Downlink transmitter with the custom-designed PCB is completed using a common ground, since they are different circuits.

3 EXPERIMENTAL RESULTS

To confirm the correct operation of the implemented communication protocols within the EIS from the Uplink receiver frontend to the Uplink receiver backend and from the Downlink transmitter backend to the Downlink transmitter frontend, the experimental set-up shown in Figure 7 was constructed. The custom-designed communication board (a) is depicted in blue, the Uplink receiver backend (b) is yellow, the Downlink transmitter frontend (c) below is green, and the analog circuit that simulates the rest of the smart PV array (d) is symbolized by orange (DC/AC converter of each Smart Photovoltaic cell, a transformer used to measure the current of the power lines in the uplink receiver, the load of the circuit, optocouplers that ensure the galvanic isolation of the two bridge circuits, filters, and a Schmitt comparator trigger).

Two FPGA development boards were used, as well as the custom PCB that composes the Uplink Receiver Backend, the Downlink Transmitter Frontend, and the network interface of the EIS. The 2

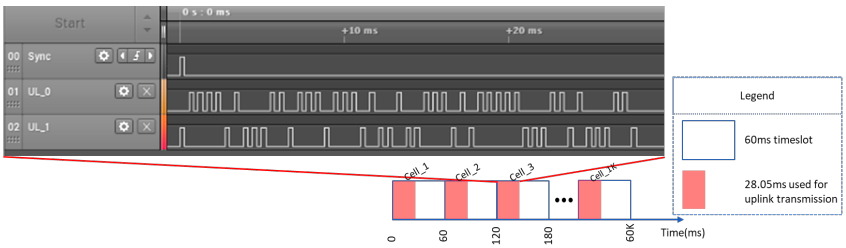

Figure 5: Example of a three-wire interface used on the Uplink interface.

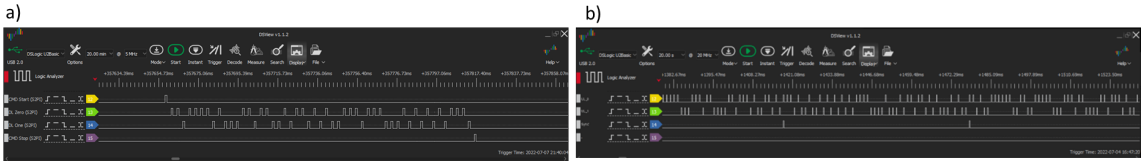

Figure 8: Measurements for the four (a) and three-wire (b) interfaces.

FPGAs carry the code of the Uplink Receiver Frontend and Downlink Transmitter Backend. In the logic analyzer plot presented in Figure 8a, the communication of the downlink interface of the smart PV element is presented, while in Figure 8b the communication of the uplink is shown.

4 DISCUSSION AND CONCLUSIONS

This paper presents the analysis and implementation of a novel two-way communication protocol, which was developed for the communication between the EIS and a Smart PV array. When compared to other implementations in the literature, the main advantage of the implemented communication system is that it is hybrid thus, it can transmit data to both AC and DC buses. This communication system will aid in the maximization and management of the energy produced by each solar cell, as well as detection and isolation of faulty PV cells, ensuring maximum energy production. The experimental results validate the feasibility and effectiveness of the proposed communication protocol between the EIS subsystems of the SmartPV array. The communication protocol not only meets the specifications for sending information from 1000 smart PV cells in one minute but also the strict timing required by the protocol for sending the 212 configuration bits to the Smart PV array's four PV strings, while accurately maintaining the required time delays between command transmission.

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